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IMAGINE 128™ I/O Information

Section 3: IMAGINE 128™ I/O Information

3.1 Signal Descriptions

IMAGINE 128™ signal pins are categorized into the following five groups: **PCI Bus Interface, Display Buffer Interface, Peripheral Devices Interface, CRT Control**, and miscellaneous. The "#" indicates an active low signal.

PCI BUS INTERFACE SIGNALS (48)

NAME	I/O	DESCRIPTION
AD[31:0]	I/O	Multiplexed address and data bus
C_BE[3:0]	I/O	Command and Byte enables
HCLK	I	Host Bus Clock
RST#	I	System Reset
FRAME#	I/O	PCI cycle FRAME
PRDY#	I/O	Processor Ready
TRDY#	I/O	Target Ready
DEVSEL#	I/O	PCI Device Select
STOP#	I/O	PCI cycle stop
INTRP#	O	Interrupt Pin
PAR	I/O	PCI Parity indicator
IDSEL	I	PCI Configuration Select
REQ#	O	Request bus mastering
GNT#	I	Grant bus mastering

DISPLAY BUFFER CONTROL SIGNALS (164)

The local memory buffers of Imagine3 may be built using one of three types of memory:

WINDOW RAM,
SGRAM,
EDO (DRAM and/or VRAM).

Names and/or function of some signals in this group change accordingly with selected type of memories.

Window RAM configuration:

NAME	I/O	DESCRIPTION
MCLK	I	Memory Controller Clock
RAD [9:0]	O	Display and Virtual Buffer Address
PDAT [127:0]	I/O	Display and Virtual Buffer Data Bus
DRAS# [3:0]	O	Display Buffer Row Address Strobes
VRAS# [1:0]	O	Virtual Buffer Row Address Strobes
BE# [15:0]	O	Display and Virtual Buffer Byte Enable
CAS# [1:0]	O	Display and Virtual Buffer Column Address Strobes
D_OE#	O	Output enable for Display Buffer
V_OE#	O	Virtual Buffer Output enable
SF[2:0]	O	Display and Virtual Buffer Special Function Signal
SOE# [3:0]	O	Display Buffer Serial Output enable

SGRAM configuration:

NAME	I/O	DESCRIPTION
MCLK	I	Memory Controller Clock
RAD [9:0]	O	Display and Virtual Buffer Address RAD[9] is used as SGRAM bank select
PDAT [127:0]	I/O	Display and Virtual Buffer Data Bus
D_CS# [3:0]	O	Display Buffer Chip Select D_SC#[3:2] are used as RAD[11:10] in case of 16Mbit SGRAM
V_CS# [1:0]	O	Virtual Buffer Chip Select D_SC#[1] is used as RAD[10] in case of 16Mbit SGRAM
DQM# [15:0]	O	Display and Virtual Buffer Byte Enable
WE# [1:0]	O	Display and Virtual Buffer Write Enable
D_SF	O	Display Buffer Special Function Signal
V_SF	O	Virtual Buffer Special Function Signal
RAS#	O	Display and Virtual Buffer Row Address Strobe Enable
CAS#	O	Display and Virtual Buffer Column Address Strobe Enable

EDO configuration:

NAME	I/O	DESCRIPTION
MCLK	I	Memory Controller Clock
RAD [9:0]	O	Display and Virtual Buffer Address
PDAT [127:0]	I/O	Display and Virtual Buffer Data Bus
DRAS# [3:0]	O	Display Buffer Row Address Strobes
VRAS# [1:0]	O	Virtual Buffer Row Address Strobes
CAS# [15:0]	O	Display and Virtual Buffer Column Address Strobes
WB_WE [1:0]	O	Display and Virtual Buffer Write-per-bit/Write Strobes
DT_OE#	O	Data Transfer / Output enable for Display Buffer
V_OE#	O	Virtual Buffer Output enable
SF[0]	O	Display Buffer Special Function Signal (VRAM)
SOE#[3:0]	O	Display Buffer Serial Output enable (VRAM)

PERIPHERAL DEVICES CONTROL SIGNALS (30)

NAME	I/O	DESCRIPTION
PA [9:0]	O	Address
PD [7:0]	I/O	Data Bus
PWE#	O	Write Strobe
POE#	O	EPROM Output Enable
PCS#	O	EPROM Chip Select
PWR#	O	Peripheral Port (DAC) Write
PRD#	O	Peripheral Port (DAC) Read
PSFT	O	Load Soft Switch

CRT CONTROLLER SIGNALS (41)

NAME	I/O	DESCRIPTION
VCLK	I	Video Timing Clock
SCLK	I/O	Serial Clock
HSYNC	O	Horizontal Sync
VSYNC	O	Vertical Sync
CBLANK	O	Composite Blank
DDC_DAT	I/O	DDC Data to/from monitor
DDC_CLK	I/O	DDC clock
EXV#	I	Enable External Video
LD_CLK	O	RAMDAC Load Clock
DDAT[31:0]	O	DRAM Controller/ VGA data

MISCELLANEOUS SIGNALS (9)

NAME	I/O	DESCRIPTION
DECLK	I	Drawing Engine Clock
RST_OUT#	O	Buffered System Reset
SENSE#	I	SENSE input (from RAMDAC)
VCSEL	0	VGA Clock Frequency Select
TOUT	O	Factory Test

3.2 Pin Assignments

IMAGINE 128™ is packaged in a 352 pin Plastic Ball Grid Array (PBGA). [There are a total of XXX signal pins and XXX power pins; six (6) five volt VDD that power the PCI I/O buffers, 28 three volt VDD that power the core and all non-PCI I/O buffers, and 28 GND pins.]

NAME	NUMBER	I/O	DRIVE (mA)
AD [31]	C10	I/O	
AD [30]	A9	I/O	
AD [29]	D8	I/O	
AD [28]	B8	I/O	
AD [27]	A7	I/O	
AD [26]	D7	I/O	
AD [25]	B7	I/O	
AD [24]	A5	I/O	
AD [23]	C6	I/O	
AD [22]	D5	I/O	
AD [21]	B5	I/O	
AD [20]	C4	I/O	
AD [19]	C5	I/O	
AD [18]	C7	I/O	
AD [17]	A3	I/O	
AD [16]	J4	I/O	
AD [15]	E4	I/O	
AD [14]	G1	I/O	
AD [13]	E3	I/O	
AD [12]	H2	I/O	
AD [11]	E1	I/O	
AD [10]	H1	I/O	
AD [09]	E2	I/O	
AD [08]	J3	I/O	
AD [07]	J2	I/O	
AD [06]	H3	I/O	
AD [05]	K1	I/O	
AD [04]	F2	I/O	
AD [03]	K2	I/O	
NAME	**NUMBER**	**I/O**	**DRIVE (mA)**

AD [02]	G3	I/O	
AD [01]	L2	I/O	
AD [00]	G4	I/O	
C_BE [3]	A6	I	
C_BE [2]	B3	I	
C_BE [1]	G2	I	
C_BE [0]	K4	I	
HCLK	C11	I	
RST#	D12	I	
FRAME#	B9	I	
PRDY#	B1	I	
TRDY#	C2	O	
DEVSEL#	C1	O	
INTRP#	C8	O	
STOP#	D1	O	
PAR	D2	O	
IDSEL	B4	O	
REQ#	C9	O	
GNT#	F3	I	
MCLK	F26	I	
RAD [9]	D18	O	12
RAD [8]	K26	O	12
RAD [7]	L26	O	12
RAD [6]	M26	O	12
RAD [5]	N26	O	12
RAD [4]	P26	O	12
RAD [3]	AE26	O	12
RAD [2]	AD26	O	12
RAD [1]	AC26	O	12
RAD [0]	AB26	O	12
PDAT [127]	R25	I/O	4
PDAT [126]	R24	I/O	4
PDAT [125]	R23	I/O	4

NAME	NUMBER	I/O	DRIVE (mA)
PDAT [124]	T24	I/O	4
PDAT [123]	T25	I/O	4
PDAT [122]	T26	I/O	4
PDAT [121]	U24	I/O	4
PDAT [120]	U23	I/O	4
PDAT [119]	AD22	I/O	4
PDAT [118]	AF23	I/O	4
PDAT [117]	AF24	I/O	4
PDAT [116]	AE22	I/O	4
PDAT [115]	AE23	I/O	4
PDAT [114]	AE24	I/O	4
PDAT [113]	AD23	I/O	4
PDAT [112]	AD25	I/O	4
PDAT [111]	AF21	I/O	4
PDAT [110]	AE21	I/O	4
PDAT [109]	AD21	I/O	4
PDAT [108]	AF20	I/O	4
PDAT [107]	AE20	I/O	4
PDAT [106]	AD20	I/O	4
PDAT [105]	AC20	I/O	4
PDAT [104]	AE19	I/O	4
PDAT [103]	AE11	I/O	4
PDAT [102]	AF11	I/O	4
PDAT [101]	AE12	I/O	4
PDAT [100]	AD12	I/O	4
PDAT [99]	AC12	I/O	4
PDAT [98]	AD13	I/O	4
PDAT [97]	AE13	I/O	4
PDAT [96]	AF14	I/O	4
PDAT [95]	AD11	I/O	4
PDAT [94]	AE10	I/O	4
PDAT [93]	AD10	I/O	4
PDAT [92]	AC9	I/O	4

NAME	NUMBER	I/O	DRIVE (mA)
PDAT [91]	AD9	I/O	4
PDAT [90]	AE9	I/O	4
PDAT [89]	AF9	I/O	4
PDAT [88]	AE8	I/O	4
PDAT [87]	AC1	I/O	4
PDAT [86]	AB2	I/O	4
PDAT [85]	AB3	I/O	4
PDAT [84]	AB4	I/O	4
PDAT [83]	AC2	I/O	4
PDAT [82]	AC3	I/O	4
PDAT [81]	AD1	I/O	4
PDAT [80]	AD2	I/O	4
PDAT [79]	AA3	I/O	4
PDAT [78]	AA2	I/O	4
PDAT [77]	AA1	I/O	4
PDAT [76]	Y4	I/O	4
PDAT [75]	Y3	I/O	4
PDAT [74]	Y2	I/O	4
PDAT [73]	W4	I/O	4
PDAT [72]	W3	I/O	4
PDAT [71]	L1	I/O	4
PDAT [70]	K3	I/O	4
PDAT [69]	L3	I/O	4
PDAT [68]	M3	I/O	4
PDAT [67]	M4	I/O	4
PDAT [66]	N1	I/O	4
PDAT [65]	N2	I/O	4
PDAT [64]	N3	I/O	4
PDAT [63]	U26	I/O	4
PDAT [62]	V25	I/O	4
PDAT [61]	V24	I/O	4
PDAT [60]	V23	I/O	4

NAME	NUMBER	I/O	DRIVE (mA)
PDAT [59]	W24	I/O	4
PDAT [58]	W25	I/O	4
PDAT [57]	Y24	I/O	4
PDAT [56]	Y25	I/O	4
PDAT [55]	AC24	I/O	4
PDAT [54]	AC25	I/O	4
PDAT [53]	AB23	I/O	4
PDAT [52]	AB24	I/O	4
PDAT [51]	AB25	I/O	4
PDAT [50]	AA24	I/O	4
PDAT [49]	AA25	I/O	4
PDAT [48]	Y26	I/O	4
PDAT [47]	AD19	I/O	4
PDAT [46]	AC19	I/O	4
PDAT [45]	AF18	I/O	4
PDAT [44]	AE18	I/O	4
PDAT [43]	AD18	I/O	4
PDAT [42]	AE17	I/O	4
PDAT [41]	AD17	I/O	4
PDAT [40]	AC17	I/O	4
PDAT [39]	AE14	I/O	4
PDAT [38]	AD14	I/O	4
PDAT [37]	AF15	I/O	4
PDAT [36]	AE15	I/O	4
PDAT [35]	AD15	I/O	4
PDAT [34]	AE16	I/O	4
PDAT [33]	AD16	I/O	4
PDAT [32]	AF17	I/O	4
PDAT [31]	AD8	I/O	4
PDAT [30]	AE7	I/O	4
PDAT [29]	AD7	I/O	4
PDAT [28]	AC7	I/O	4

NAME	NUMBER	I/O	DRIVE (mA)
PDAT [27]	AD6	I/O	4
PDAT [26]	AE6	I/O	4
PDAT [25]	AF6	I/O	4
PDAT [24]	AE5	I/O	4
PDAT [23]	AF2	I/O	4
PDAT [22]	AF3	I/O	4
PDAT [21]	AE3	I/O	4
PDAT [20]	AD4	I/O	4
PDAT [19]	AE4	I/O	4
PDAT [18]	AF4	I/O	4
PDAT [17]	AC5	I/O	4
PDAT [16]	AD5	I/O	4
PDAT [15]	W2	I/O	4
PDAT [14]	W1	I/O	4
PDAT [13]	V3	I/O	4
PDAT [12]	V2	I/O	4
PDAT [11]	V1	I/O	4
PDAT [10]	U4	I/O	4
PDAT [09]	U3	I/O	4
PDAT [08]	U2	I/O	4
PDAT [07]	P3	I/O	4
PDAT [06]	P4	I/O	4
PDAT [05]	R2	I/O	4
PDAT [04]	R3	I/O	4
PDAT [03]	R4	I/O	4
PDAT [02]	T1	I/O	4
PDAT [01]	T2	I/O	4
PDAT [00]	T3	I/O	4
D_CS#[3] (SGRAM) DRAS# [3] (WRAM, EDO)	N25	O	6
D_CS#[2] (SGRAM) DRAS# [2] (WRAM, EDO)	L25	O	6

D_CS#[1] (SGRAM) DRAS# [1] (WRAM, EDO)	D26	O	6

NAME	NUMBER	I/O	DRIVE (mA)
D_CS#[0] (SGRAM) DRAS# [0] (WRAM, EDO)	J26	O	6
V_CS#[1] (SGRAM) VRAS# [1] (WRAM, EDO)	E25	O	6
V_CS#[0] (SGRAM) VRAS# [0] (WRAM, EDO)	U25	O	6
DQM[15] (SGRAM) BE#[15] (WINRAM) CAS# [15] (EDO)	R26	O	6
DQM[14] (SGRAM) BE#[14] (WINRAM) CAS# [14] (EDO)	AA26	O	6
DQM[13] (SGRAM) BE#[13] (WINRAM) CAS# [13] (EDO)	AF22	O	6
DQM[12] (SGRAM) BE#[12] (WINRAM) CAS# [12] (EDO)	AF13	O	6
DQM[11] (SGRAM) BE#[11] (WINRAM) CAS# [11] (EDO)	AF10	O	6
DQM[10] (SGRAM) BE#[10] (WINRAM) CAS# [10] (EDO)	AF5	O	6
DQM[09] (SGRAM) BE#[09] (WINRAM) CAS# [09] (EDO)	AB1	O	6

DQM[08] (SGRAM) BE#[08] (WINRAM) CAS# [08] (EDO)	P1	O	6
DQM[07] (SGRAM) BE#[07] (WINRAM) CAS# [07] (EDO)	V26	O	6
DQM[06] (SGRAM) BE#[06] (WINRAM) CAS# [06] (EDO)	W26	O	6
DQM[05] (SGRAM) BE#[05] (WINRAM) CAS# [05] (EDO)	AF19	O	6
DQM[04] (SGRAM) BE#[04] (WINRAM) CAS# [04] (EDO)	AF16	O	6
DQM[03] (SGRAM) BE#[03] (WINRAM) CAS# [03] (EDO)	AF8	O	6
DQM[02] (SGRAM) BE#[02] (WINRAM) CAS# [02] (EDO)	AF7	O	6
DQM[01] (SGRAM) BE#[01] (WINRAM) CAS# [01] (EDO)	Y1	O	6
DQM[00] (SGRAM) BE#[00] (WINRAM) CAS# [00] (EDO)	U1	O	6

WE [1] (SGRAM) CAS# [1] (WINRAM) WB_WE [1] (EDO)	AF12	O	8
WE [0] (SGRAM) CAS# [0] (WINRAM) WB_WE [0] (EDO)	P25	O	8
D_SF (SGRAM) D_OE# (WINRAM) DT_OE# (EDO)	H26	O	8
V_SF (SGRAM) V_OE# (WINRAM) V_OE# (EDO)	AC22	O	8
CAS# (SGRAM) SF[2] (WINRAM) (EDO N/A)	M23	O	12
RAS# (SGRAM) SF[1] (WINRAM) (EDO N/A)	Y23	O	12
(SGRAM N/A) SF[0] (WINRAM) SF[0] (EDO)	F24	O	12
(SGRAM N/A) SOE[3]# (WINRAM, EDO)	R1	O	2
(SGRAM N/A) SOE[2]# (WINRAM, EDO)	P2	O	2

(SGRAM N/A) SOE[1]# (WINRAM, EDO)	M2	O	2
(SGRAM N/A) SOE[0]# (WINRAM, EDO)	M1	O	2
PA [9]	C16	O	2
PA [8]	C17	O	2
PA [7]	A10	O	2
PA [6]	B11	O	2
PA [5]	A11	O	2
PA [4]	B12	O	2
PA [3]	A12	O	2
PA [2]	B13	O	2
PA [1]	A13	O	2
PA [0]	B14	O	2

NAME	NUMBER	I/O	DRIVE (mA)
PD [07]	A18	I/O	4
PD [06]	A17	I/O	4
PD [05]	B17	I/O	4
PD [04]	A16	I/O	4
PD [03]	B16	I/O	4
PD [02]	A15	I/O	4
PD [01]	B15	I/O	4
PD [00]	A14	I/O	4
PWE#	C26	O	2
POE#	E26	O	2
VCLK	B23	I	
SCLK	G26	I/O	8
HSYNC	B24	O	4
VSYNC	A24	O	4
CBLANK	A23	O	4
DECLK	K25	I	
SENSE#	A22	I	
RST_OUT#	B21	O	2
PWR#	D20	O	2
PRD#	C21	O	2
PCS#	B22	O	2
PSFT	C15	O	2

NAME	NUMBER	I/O	DRIVE (mA)
EXV#	B10	I	
DDC_DAT	A25	I/O	4
DDC2_CLK	B20	I/O	4
VCSEL	C20	O	4
LD_CLK	A21	O	4
DDAT[31]	B18	O	4
DDAT[30]	C18	O	4
DDAT[29]	A19	O	4
DDAT[28]	A20	O	4
DDAT[27]	B19	O	4
DDAT[26]	C19	O	4
DDAT[25]	C22	O	4
DDAT[24]	D22	O	4
DDAT[23]	C23	O	4
DDAT[22]	H23	O	4
DDAT[21]	D17	O	4
DDAT[20]	C25	O	4
DDAT[19]	D24	O	4
DDAT[18]	D25	O	4
DDAT[17]	E24	O	4
DDAT[16]	E23	O	4
DDAT[15]	F25	O	4
DDAT[14]	G25	O	4
DDAT[13]	G23	O	4
DDAT[12]	G24	O	4
DDAT[11]	H25	O	4
DDAT[10]	H24	O	4
DDAT[9]	J25	O	4
DDAT[8]	J24	O	4
DDAT[7]	K24	O	4
DDAT[6]	K23	O	4
DDAT[5]	L24	O	4

NAME	NUMBER	I/O	DRIVE (mA)
DDAT[4]	M25	O	4
DDAT[3]	M24	O	4
DDAT[2]	N23	O	4
DDAT[1]	N24	O	4
DDAT[0]	P24	O	4
TOUT	AC10	O	4

Power Pins

NAME	NUMBER
VDD (+5 volts)	A4, A8, B6, D3, F1, J1
VDD (+3 volts)	D6, D11, D16, D21, F4, F23, L4, L23, T4, T23, AA4, AC6, AC11, AC16, AC21, AA23
VSS	A1, A2, A26, B2, B25, B26, C3, C12, C13, C14, C24, D4, D9, D13, D14, D15, D19, D23, H4, J23, N4, P23, V4, W23, AC4, AC8, AC13, AC14, AC15, AC18, AC23, AD3, AD24, AE1, AE2, AE25, AF1, AF25, AF26

Note: D10 and all pins N/C or N/A are unconnected pins.

3.2.1 Imagine 3 128™ Bottom View

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26
AF	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O
	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51
AE	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O
	25	124	125	126	127	128	129	130	131	132	133	134	135	136	137	138	139	140	141	142	143	144	145	146	147	52
AD	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O
	24	123	214	215	216	217	218	219	220	221	222	223	224	225	226	227	228	229	230	231	232	233	234	235	148	53
AC	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O
	23	122	213	296	297	298	299	300	301	302	303	304	305	306	307	308	309	310	311	312	313	314	315	236	149	54
AB	O	O	O	O																			O	O	O	O
	22	121	212	295																			316	237	150	55
AA	O	O	O	O																			O	O	O	O
	21	120	211	294																			317	238	151	56
Y	O	O	O	O																			O	O	O	O
	20	119	210	293																			318	239	152	57
W	O	O	O	O																			O	O	O	O
	19	118	209	292																			319	240	153	58
V	O	O	O	O																			O	O	O	O
	18	117	208	291																			320	241	154	59
U	O	O	O	O																			O	O	O	O
	17	116	207	290																			321	242	155	60
T	O	O	O	O																			O	O	O	O
	16	115	206	289																			322	243	156	61
R	O	O	O	O																			O	O	O	O
	15	114	205	288																			323	244	157	62
P	O	O	O	O																			O	O	O	O
	14	113	204	287																			324	245	158	63
N	O	O	O	O																			O	O	O	O
	13	112	203	286																			325	246	159	64
M	O	O	O	O																			O	O	O	O
	12	111	202	285																			326	247	160	65
L	O	O	O	O																			O	O	O	O
	11	110	201	284																			327	248	161	66
K	O	O	O	O																			O	O	O	O
	10	109	200	283																			328	249	162	67
J	O	O	O	O																			O	O	O	O
	9	108	199	282																			329	250	163	68
H	O	O	O	O																			O	O	O	O
	8	107	198	281																			330	251	164	69
G	O	O	O	O																			O	O	O	O
	7	106	197	280																			331	252	165	70
F	O	O	O	O																			O	O	O	O
	6	105	196	279																			332	253	166	71
E	O	O	O	O																			O	O	O	O
	5	104	195	278																			333	254	167	72
D	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O
	4	103	194	277	352	351	350	349	348	347	346	345	344	343	342	341	340	339	338	337	336	335	334	255	168	73
C	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O
	3	102	193	276	275	274	273	272	271	270	269	268	267	266	265	264	263	262	261	260	259	258	257	256	169	74
B	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O
	2	101	192	191	190	189	188	187	186	185	184	183	182	181	180	179	178	177	176	175	174	173	172	171	170	75
A	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O
	1	100	99	98	97	96	95	94	93	92	91	90	89	88	87	86	85	84	83	82	81	80	79	78	77	76
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26

3.3 EDO Configuration (Top View)

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	W	Y	AA	AB	AC	AD	AE	AF	
26	GND	GND	PWE#	DRAS#1	POE#	MCLK	SCLK	DT_OE#	DRAS#0	RAD8	RAD7	RAD6	RAD5	RAD4	CAS#15	PDAT127	PDAT123	PDAT63	CAS#07	CAS#06	PDAT48	CAS#14	RAD0	RAD1	RAD2	RAD3	GND	26
25	DDC_DAT	GND	DDAT20	DDAT18	VRAS#1	DDAT15	DDAT14	DDAT11	DDAT9	DECLK	DRAS#2	DDAT4	DRAS#3	WB_WE3	PDAT127	PDAT125	VRAS#0	PDAT62	PDAT58	PDAT56	PDAT49	PDAT51	PDAT54	PDAT112	GND	GND	25
24	VSYNC	HSYNC	GND	DDAT19	DDAT17	N/C	DDAT12	DDAT10	DDAT8	DDAT7	DDAT5	DDAT3	DDAT1	DDAT0	PDAT126	PDAT124	PDAT121	PDAT61	PDAT59	PDAT57	PDAT50	PDAT52	PDAT55	GND	PDAT114	PDAT117	24
23	CBLANK	VCLK	DDAT23	GND	DDAT16	VDD3	DDAT13	DDAT22	GND	DDAT6	VDD3	N/C	DDAT2	GND	PDAT125	VDD3	PDAT120	PDAT60	GND	N/C	VDD3	PDAT53	GND	PDAT113	PDAT115	PDAT116	23
22	SENSE#	PCS#	DDAT25	DDAT24																			V_OE#	PDAT119	PDAT118	CAS#13	22
21	LD_CLK	RST_OUT#	PRD#	VDD3																			VDD3	PDAT109	PDAT110	PDAT111	21
20	DDAT28	DDC2_CLK	VCSEL	PWR#																			PDAT105	PDAT106	PDAT107	PDAT108	20
19	DDAT29	DDAT27	DDAT26	GND																			PDAT46	PDAT47	PDAT104	CAS#05	19
18	PD07	DDAT31	DDAT30	RAD9																			GND	PDAT43	PDAT44	PDAT45	18
17	PD06	PD05	PA8	DDAT21																			PDAT40	PDAT41	PDAT42	PDAT32	17
16	PD04	PD03	PA9	VDD3																			VDD3	PDAT33	PDAT34	CAS#04	16
15	PD02	PD01	PSFT	GND																			GND	PDAT35	PDAT36	PDAT37	15
14	PD00	PA0	GND	GND																			GND	PDAT38	PDAT39	PDAT96	14
13	PA1	PA2	GND	GND																			GND	PDAT98	PDAT97	CAS#12	13
12	PA3	PA4	GND	RST#																			PDAT99	PDAT100	PDAT101	WB_WE1	12
11	PA5	PA6	HCLK	VDD3																			VDD3	PDAT95	PDAT103	PDAT102	11
10	PA7	EXV#	AD31	N/C																			TOUT	PDAT93	PDAT94	CAS#11	10
9	AD30	FRAME#	REQ#	GND																			PDAT92	PDAT91	PDAT95	PDAT89	9
8	VDD5	AD28	INTRP#	AD29																			GND	PDAT31	PDAT88	CAS#03	8
7	AD27	AD25	AD18	AD26																			PDAT28	PDAT29	PDAT30	CAS#02	7
6	C_BE3	VDD5	AD23	VDD3																			VDD3	PDAT27	PDAT26	PDAT25	6
5	AD24	AD21	AD19	AD22																			PDAT17	PDAT16	PDAT24	CAS#10	5
4	VDD5	IDSEL	AD20	GND	AD15	VDD3	AD00	GND	AD16	C_BE0	VDD3	PDAT67	GND	PDAT06	PDAT03	VDD3	PDAT10	GND	PDAT73	PDAT76	VDD3	PDAT84	GND	PDAT20	PDAT19	PDAT18	4
3	AD17	C_BE2	GND	VDD5	AD13	GNT#	AD02	AD06	AD08	PDAT70	PDAT69	PDAT68	PDAT64	PDAT07	PDAT04	PDAT00	PDAT09	PDAT13	PDAT72	PDAT75	PDAT79	PDAT85	PDAT82	GND	PDAT21	PDAT22	3
2	GND	GND	TRDY#	PAR	AD09	ADD4	C_BE1	AD12	AD07	AD03	AD01	SOE1#	PDAT65	SOE2#	PDAT05	PDAT01	PDAT08	PDAT12	PDAT15	PDAT74	PDAT78	PDAT86	PDAT83	PDAT80	GND	PDAT23	2
1	GND	PRDY#	DEVSEL#	STOP#	AD11	VDD5	AD14	AD10	VDD5	AD05	PDAT71	SOE0#	PDAT66	CAS#08	SOE3#	PDAT02	CAS#00	PDAT11	PDAT14	CAS#01	PDAT77	CAS#09	PDAT87	PDAT81	GND	GND	1
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	W	Y	AA	AB	AC	AD	AE	AF	

Imagine128 Series 3 (EDO MEMORY)

352 PBGA (Top View)

Revision 1.0

Date: November 18, 1996

S.W.C.

3.4 SGRAM Configuration (Top View)

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	W	Y	AA	AB	AC	AD	AE	AF	
26	GND	GND	PWE#	D_CS#1	PDE#	MCLK	*See Note	D_SF	D_CS#0	RAD5	RAD7	RAD6	RAD5	RAD4	DQM1S	PDAT122	PDAT63	DQM07	DQM06	PDAT48	DQM14	RAD0	RAD1	RAD2	RAD3	GND	26
25	DDC_DAT	GND	DDAT20	DDAT18	V_CS#1	DDAT15	DDAT14	DDAT11	DDAT9	DECLK	D_CS#2	DDAT4	D_CS#3	WE0	PDAT127	PDAT125	V_CS#0	PDAT62	PDAT58	PDAT56	PDAT49	PDAT51	PDAT54	PDAT112	GND	GND	25
24	VSYNC	HSYNC	GND	DDAT19	DDAT17	N/C	DDAT12	DDAT10	DDAT8	DDAT7	DDAT5	DDAT3	DDAT1	DDAT0	PDAT126	PDAT124	PDAT123	PDAT61	PDAT59	PDAT57	PDAT50	PDAT52	PDAT55	GND	PDAT113	PDAT114	PDAT115	24
23	CBLANK	VCLK	DDAT23	GND	DDAT16	VDD3	DDAT13	DDAT22	GND	DDAT6	VDD3	CAS#	DDAT2	GND	PDAT125	VDD3	PDAT120	PDAT60	GND	RAS#	VDD3	PDAT53	GND	PDAT116	PDAT117	PDAT118	23
22	SENSE#	PCS#	DDAT26	DDAT24																			V_SF	PDAT119	PDAT119	DQM15	22
21	LD_CLK	RST_OUT#	PRD#	VDD3																			VDD3	PDAT109	PDAT110	PDAT111	21
20	DDAT28	DDC2_CLK	VCSEL	PWR#																			PDAT105	PDAT106	PDAT107	PDAT108	20
19	DDAT29	DDAT27	DDAT26	GND																			PDAT46	PDAT47	PDAT104	DQM05	19
18	PD07	DDAT31	DDAT30	RAD9																			GND	PDAT43	PDAT44	PDAT45	18
17	PD06	PD05	PA8	DDAT21																			PDAT40	PDAT41	PDAT42	PDAT32	17
16	PD04	PD03	PA9	VDD3																			VDD3	PDAT33	PDAT34	DQM04	16
15	PD02	PD01	PSFT	GND																			GND	PDAT35	PDAT36	PDAT37	15
14	PD00	PA0	GND	GND																			GND	PDAT38	PDAT39	PDAT96	14
13	PA1	PA2	GND	GND																			GND	PDAT98	PDAT97	DQM12	13
12	PA3	PA4	GND	RST#																			PDAT99	PDAT100	PDAT101	WE1	12
11	PA5	PA6	HCLK	VDD3																			VDD3	PDAT95	PDAT103	PDAT102	11
10	PA7	EXV#	AD31	N/C																			TOUT	PDAT93	PDAT94	DQM11	10
9	AD30	FRAME#	REQ#	GND																			PDAT92	PDAT91	PDAT90	PDAT89	9
8	VDD5	AD28	INTR9#	AD29																			GND	PDAT31	PDAT88	DQM03	8
7	AD27	AD25	AD18	AD26																			PDAT28	PDAT29	PDAT30	DQM02	7
6	C_BE3	VDD5	AD23	VDD3																			VDD3	PDAT27	PDAT26	PDAT25	6
5	AD24	AD21	AD19	AD22																			PDAT17	PDAT16	PDAT24	DQM10	5
4	VDD5	IDSEL	AD20	GND	AD15	VDD3	AD00	GND	AD16	C_BE0	VDD3	PDAT67	GND	PDAT96	PDAT93	VDD3	PDAT10	GND	PDAT73	PDAT76	VDD3	PDAT94	GND	PDAT20	PDAT19	PDAT18	4
3	AD17	C_BE2	GND	VDD5	AD13	ONT#	AD02	AD06	AD08	PDAT70	PDAT69	PDAT68	PDAT64	PDAT97	PDAT94	PDAT93	PDAT09	PDAT13	PDAT72	PDAT75	PDAT79	PDAT85	PDAT82	GND	PDAT21	PDAT22	3
2	GND	GND	TRDY#	PAR	AD09	AD04	C_BE1	AD12	AD07	AD03	AD01	N/C	PDAT65	N/C	PDAT85	PDAT81	PDAT08	PDAT12	PDAT15	PDAT74	PDAT78	PDAT86	PDAT83	PDAT80	GND	PDAT23	2
1	GND	PRDY#	DEVSEL#	STOP#	AD11	VDD5	AD14	AD10	VDD5	AD05	PDAT71	N/C	PDAT66	DQM08	N/C	PDAT92	DQM00	PDAT11	PDAT14	DQM01	PDAT77	DQM09	PDAT87	PDAT81	GND	GND	1
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	W	Y	AA	AB	AC	AD	AE	AF	

Imagine128 Series 3 (SGRAM MEMORY)

352 PBGA (Top View)

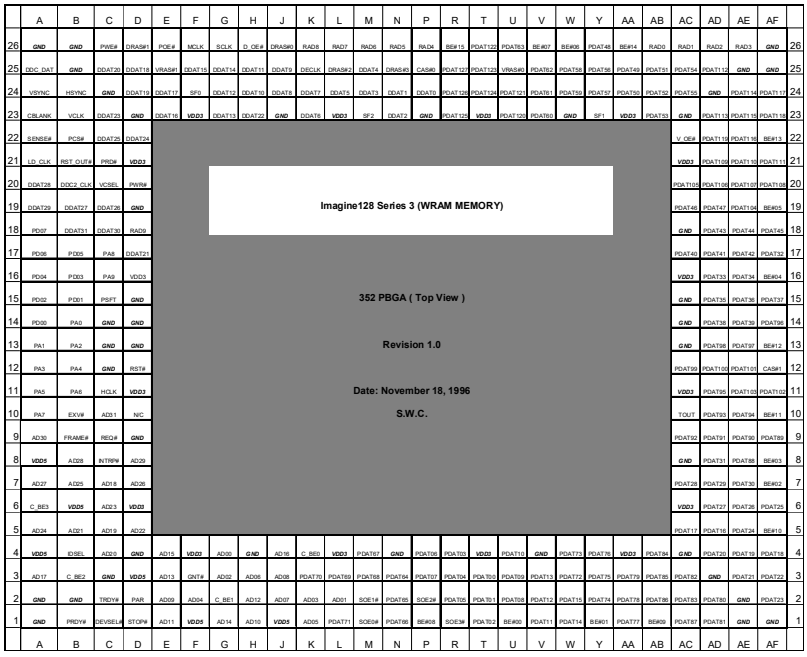
Revision 1.0

Date: November 18, 1996

S.W.C.

* Note: Unused I/O. Tie to Resistor to GND.

3.5 WINDOW RAM Configuration (Top View)



3.6 Configuration Pins

As IMAGINE 128™ is being reset during the power up sequence, the logic states of pins PDAT[76:0] are used to configure specific functions. These pins are internally pulled down to logic zero. A value of logic one can be achieved on any of the configuration pins through the use of an external pull up resistor. The values on PDAT[76:0] are latched into IMAGINE 128™ on the rising edge of the RST# signal and may be read at any time in the ID or CONFIG registers. The notation "CJ[0]" corresponds to the logic state on PDAT[0] at the rising edge of RST#. Likewise, CJ[37:36] would correspond to PDAT[37:36].

Добавлено примечание ([NNCC1]):

PINS	NAME	VALUE	DESCRIPTION
CJ[1:0]	BASE0		PCI Base 0 Address Register Size
		00	4 Megabyte Memory Space Requested
		01	8 Megabyte Memory Space Requested
		10	16 Megabyte Memory Space Requested
		11	32 Megabyte Memory Space Requested
CJ[3:2]	BASE1		PCI Base 1 Address Register Size
		00	4 Megabyte Memory Space Requested
		01	8 Megabyte Memory Space Requested
		10	16 Megabyte Memory Space Requested
		11	32 Megabyte Memory Space Requested
CJ[5:4]	BASE2		PCI Base 2 Address Register Size
		00	4 Megabyte Memory Space Requested
		01	8 Megabyte Memory Space Requested
		10	16 Megabyte Memory Space Requested
		11	32 Megabyte Memory Space Requested
CJ[7:6]	BASE3		PCI Base 3 Address Register Size
		00	4 Megabyte Memory Space Requested
		01	8 Megabyte Memory Space Requested
		10	16 Megabyte Memory Space Requested
		11	32 Megabyte Memory Space Requested
CJ[10:8]	BASEROM		PCI EPROM Base Address Register Size
		0x0	32 Kilobyte Memory Space Requested
		0x1	64 Kilobyte Memory Space Requested
		0x2	128 Kilobyte Memory Space Requested
		0x3	256 Kilobyte Memory Space Requested
		0x4	512 Kilobyte Memory Space Requested
		0x5	1 Megabyte Memory Space Requested
		0x6	2 Megabyte Memory Space Requested
		0x7	2 Megabyte Memory Space Requested

Configuration Pins (Continued)

PINS	NAME	VALUE	DESCRIPTION
CJ[26:25]	DDEN		Display buffer memory density
		00	No memory present
		01	256K bits by N memory chips
		10	Reserved for WINRAM and EDO 512K bits by 32 (SGRAM 16 MB only)
		11	Reserved
CJ[27]	DB[0]		Number of banks in Display buffer. This bit is used in conjunction with CJ[43] see note 1*)
CJ[29:28]	VDEN		Virtual buffer memory density
		00	No memory present
		01	256K bits by N memory chips
		10	1M bit by N (for EDO only) 512K bits by 32 (SGRAM 16 MB only)
		11	Reserved
CJ[30]	VB		Number of banks in Virtual buffer
		0	One bank
		1	Two banks
CJ[33]	TRAL		Extend RAS low time during write cycle (see timing diagram for EDO memory)
		0	Normal timing
		1	Extended timing
			In SGRAM and Window RAM it is a “don’t care” bit.
CJ[34]	INT_EN		Interrupt Line Enable
		0	Disable IMAGINE 128® Interrupt generation
		1	Enable IMAGINE 128® Interrupt generation
CJ[35]	SGR		SGRAM select. This bit is used in conjunction with CJ[49] and can be read in CONFIG2 register.
		0	see *note 2)
		1	

Configuration Pins (Continued)

PINS	NAME	VALUE	DESCRIPTION
CJ[37:36]	CLASS		PCI Device Sub-Class
		00	VGA
		01	XGA
		10	Other
		11	Other
CJ[38]	EE		EPROM Enable: This signal is the master EPROM enable signal. If this signal is not asserted, then all EPROM access will be disabled regardless of the state of the PCI EPROM enable bit in the EPROM base register.
		0	EPROM Decode disabled
		1	EPROM Decode Enabled
CJ[39]	DS		IMAGINE 128™ Pixel Data Bus Size: This pin specifies the actual pixel bus width. This bit is shadowed to the "one28" bit in the CONFIG1 register.
		0	64 bit pixel data bus
		1	128 bit pixel data bus
CJ[40]	SPARE		This Configuration Jumper does not affect any function within IMAGINE 128™. It can be used to provide board specific information and can be read from bit[4] of the CONFIG1 register.
CJ[41]	FBB		Fast Back-to-Back Transfer Enable This bit determines whether BLACKBIRD supports fast back-to-back transfers. It is can be read from bit[23] of the PCI Status Register or bit[24] of CONFIG2
		0	Fast Back-to-Back Transfers are not supported
		1	Fast Back-to-Back Transfers are supported

Configuration Pins (Continued)

PINS	NAME	VALUE	DESCRIPTION
CJ[42]	SPARE		This Configuration Jumper does not affect any function within IMAGINE 128™. It can be used to provide board specific information and can be read from bit[25] of the CONFIG2 register.
CJ[43]	DB[1]		Number of banks in Display buffer. This bit is used in conjunction with CJ[27] and can be read in ID register see note 1*)
CJ[44]	CONT		Continuous Memory Cycle Enable This bit determines whether IMAGINE 128™ will concatenate multiple memory request that fall within the same row into a single memory cycle. CONT can be read from bit[27] of CONFIG2
		0	All new memory requests result in RAS precharge
		1	New memory request may be combined
CJ[45]	SPARE		This Configuration Jumper does not affect any function within IMAGINE 128™. It can be used to provide board specific information and can be read from bit[28] of the CONFIG2 register.
CJ[46]	PRE		Linear Memory Windows Pre-fetch This jumper determines whether linear memory windows are pre-fetchable. All other IMAGINE 128™ resources are not pre-fetchable.
		1	Linear Memory Windows are pre-fetchable
		0	Linear Memory Windows are not pre-fetchable
CJ[48:47]	SPARE		These Configuration Jumpers do not affect any function within IMAGINE 128™. They can be used to provide board specific information and can be read from bits[31:30] of the CONFIG2 register.

Configuration Pins (Continued)

PINS	NAME	VALUE	DESCRIPTION
CJ[49]	EDO		EDO Memory Select. This bit is used in conjunction with CJ[35] and can be read in CONFIG2 register
		0 1	See note 2*) below.
CJ[50]	JV		Joint Transfers This bit enables serial port read transfers to occur in all banks of Display buffer, regardless of the highest order address bit. The value of this bit can be read from bit[3] of CONFIG2
		0 1	Transfer cycles are generated to a single bank of Display buffer Transfer cycles are generated to all banks of Display buffer.
			This bit has a meaning with dual ported memories only (VRAM or WINDOW RAM).
CJ[51]	TRCD		RAS to CAS delay select This bit adjusts the timing between the falling edge of RAS and the falling edge of CAS. The value of this bit can be read from bit[4] of CONFIG2.
		0 1	
			See timing diagrams for EDO and /or SGRAM cycles This bit must be set to 1 for WINDOW RAM memories.
CJ[53:52]	REF_CNT		Refresh Count Select These two bits select how often DRAM refresh cycles are generated. The value of these bits can be read from bits[6:5] of CONFIG2
		00 01 10 11	Generate DRAM refresh after 768 mclock periods Generate DRAM refresh after 1024 mclock periods Generate DRAM refresh after 1280 mclock periods Generate DRAM refresh after 3584 mclock periods

Configuration Pins (Continued)

PINS	NAME	VALUE	DESCRIPTION
CJ[70:55]	SVID		Subsystem Vendor ID This 16 bit field is the PCI Subsystem Vendor ID. It can be read at address 0x2C in PCI configuration space. This field will correspond to CJ[70:55] unless CJ[76] is set to zero, in which case the SVID will be set to 0x105D; the vendor ID for Number Nine Visual Technology
CJ[75:71]	SID		Subsystem ID This 5 bit field corresponds to the lower 5 bits of the PCI Subsystem ID; the upper 11 bits of the SID will always be zero. It can be read at address 0x2E in PCI configuration space. This field will correspond to CJ[75:71] unless CJ[76] is set to zero, in which case SID will be set to 0.
CJ[76]	SSEL		Subsystem ID Select This bit allows the Subsystem ID and Vendor ID fields in PCI configuration space to be set according to CJ[75:55].
		0	Subsystem Vendor ID = 0x105D; Subsystem ID =0
		1	Subsystem ID and Vendor ID selected by CJ[75:55]

*note 1)

CJ[43] and CJ[27] should be strapped according to number of banks in the display buffer (each bank is 4MB).
Resulting value of DB[1:0] should match the number of bank as follows:
DB[1:0] = 00 Display buffer consist of one bank
DB[1:0] = 01 Display buffer consist of two banks
DB[1:0] = 10 Display buffer consist of three banks
DB[1:0] = 11 Display buffer consist of four banks

*note 2)
CJ[49] and CJ[35] should be strapped according to the type of memory in local buffers
Corresponding bits: EDO and SGR will force memory controller to generate memory cycles as follows:
EDO=1, SGR= "don't care": => generate timing for traditional EDO memories (DRAM and/or VRAM)
EDO=0, SGR= 1 : => generate timing for SGRAM memories
EDO=0, SGR= 0 : => generate timing for WINDOW RAM memories