Appendix A

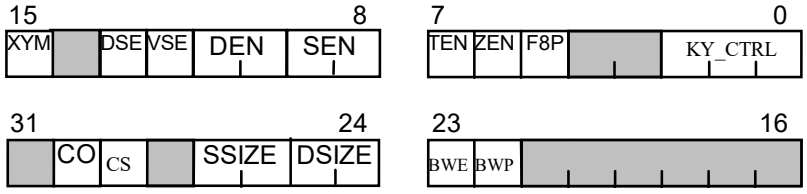
Imagine 128® Theory of Operation

Appendix A: IMAGINE 128™ Theory of Operation

A.1 Buffer Control

Control of IMAGINE 128™s three memory buffers is achieved through four buffer control registers. Each linear memory window has a buffer control register (MW0_CTRL, MW1_CTRL) and each drawing engine has a buffer control register (BUF_CTRL). The parameters in a specific buffer control register apply only to the resource associated with that register. For example, MW0_CTRL has no affect on how the drawing engine or the other memory window access the three buffers.

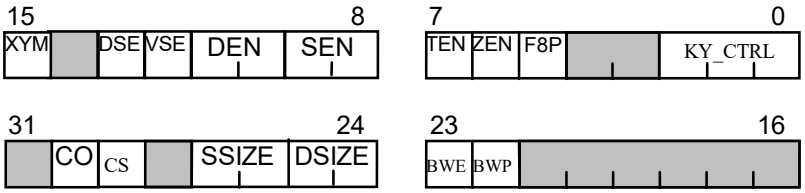
The buffer control registers for a linear window and a drawing engine are slightly different, but the drawing engine buffer control register shown below will illustrate all possible buffer control functions.



The **Source Enable** field (SEN) determines whether the internal cache or one of the three buffers is the source of data during a read cycle. The **Destination Enable** field (DEN) determines which of the three buffers is the destination of data during a write or read-modify-write cycle.

During write or read-modify-write cycles, multiple destinations may be enabled for writing. This operation is known as write shadowing. To achieve shadowing, DEN is first set to the appropriate buffer. One or both of the other two buffers may then be enabled for writing by setting the Shadow Enable bit corresponding to the buffer(s) to be shadowed. The two shadow enable bits are VSE and DSE. They enable shadowing to the Virtual and Display Buffers respectively. Setting the shadow enable bit for a buffer that is already specified in DEN will have no effect. During a read-modify-write cycle, the source data will be read from the buffer specified by DEN.

Buffer Control (Continued)



The **CO** bit is useful when consecutive commands within a group of commands are using the cache as the source of data. To use the CO bit, one programs the appropriate drawing engine registers, loads the cache with data, and then triggers the command by writing XY1. The drawing engine will execute the command without interruption. This technique is useful when one wants to partition the cache into halves. The drawing engine can be executing from one half of the cache while new data for the next command is written into the other half of the cache. The CO bit essential indicates to the drawing engine that the cache will always contain valid data. CO is not reset by the drawing engine.

The **CS** bit is used to select cache writing between XY windows and the texel cache/ palette.

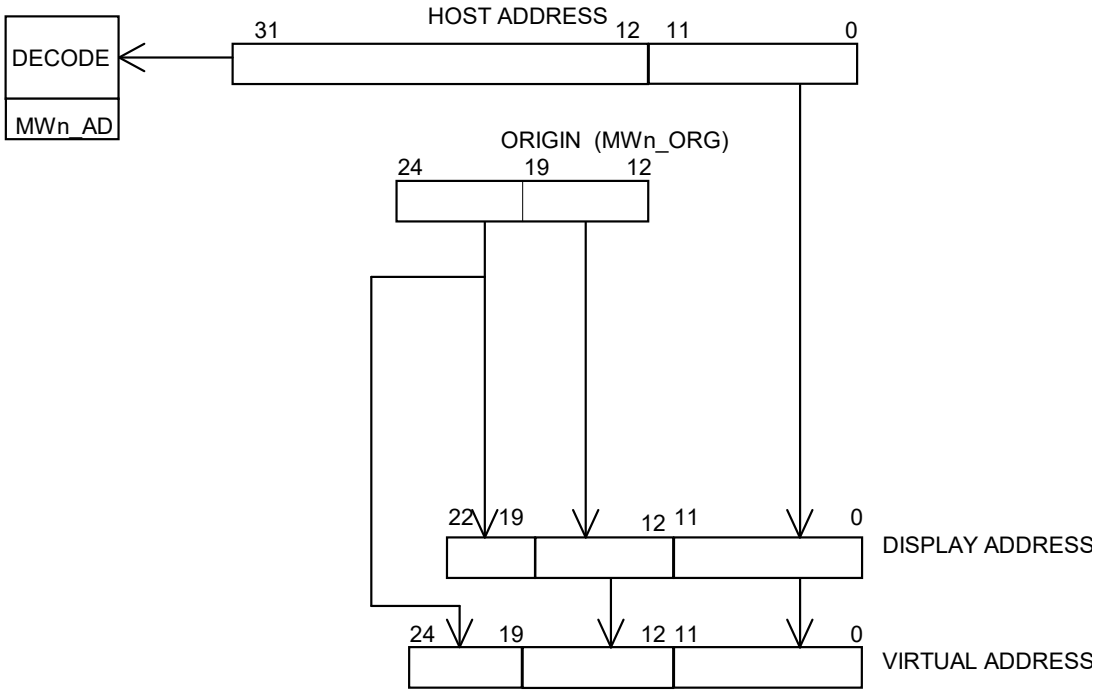
A.2 Linear Memory Windows Operation

A Linear Memory Window is defined as a region of system memory that is mapped to IMAGINE 128® local memory space. IMAGINE 128® supports two memory windows. The address in system memory space to be mapped is programmed into MWn_AD, where n=0 or 1 for memory window 0 or memory window 1. The size of the memory window is programmed into MWn_SZ. Memory windows may be programmed from 4 Kbytes to 32 Mbytes. A memory window must begin on an address boundary equal to its size. For example, a 4 Kbyte window can be start at any 4 Kbyte address while a 1 Mbyte window must begin on a 1 megabyte boundary.

The memory window can be mapped to any of IMAGINE 128® 's local buffers as described in the previous section. The address in the local buffer to which the memory window is mapped is determined by the MWn_ORG and MWn_PGE registers. The MWn_ORG register determines the starting address of the memory window in local memory space. The MWn_PGE register allows the value in MWn_ORG to be offset from 0 to 31 megabytes. A linear memory window is enabled by setting the appropriate window enable bit (EW0 or EW1) in the CONFIG1 register.

An example of how the local buffer address is calculated for a 4 Kbyte window is shown below. As can be seen from the diagram, host address bits [31:12] are compared with bits [31:12] of the MWn_AD register. If all bits are a match, this access is considered a window hit. The Virtual and Display buffer address is then generated by adding the DVPGE register to MWn_ORG[24:19] and replacing the lower twelve bits of the result with the lower twelve bits of the host address. If masking isn't enabled, the mask address calculation is the same with the exception that the MPGE bits from the MWn_PGE register are added to MWn_ORG[23:19]. With masking enabled, the mask address is equal to MWn_MSRC concatenated with the lower twelve bits of the host address.

ADDRESS FLOW FOR 4K BYTE MEMORY WINDOW



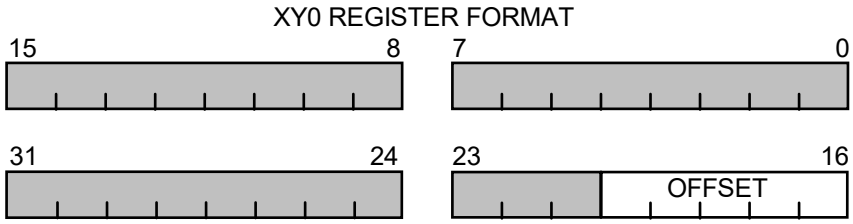
A.3 X-Y Windows Operation

An X-Y Memory Window maps a region of system memory into an X-Y oriented local memory space. The biggest architectural difference between Linear and X-Y memory windows is that a linear memory window completely bypasses the drawing pipeline while an X-Y window passes thorough the drawing pipeline. Data is transferred through an X-Y window by using the drawing engine's Read Transfer (RXFER) and Write Transfer (WXFER) command.

To set up an X-Y window, the X-Y window address (XYW_AD) must be initialized. XYW_AD defines the region of system memory space that will be decoded as an X-Y window. The SIZE field within XYW_AD determines how much system address space will be mapped to the X-Y window. As with a linear window, the size of the X-Y window determines on what address boundary the window may begin. The X-Y window decode is enabled by setting the X-Y window enable bit (EXA) in the CONFIG1 register.

A.3.1 XY Registers for X-Y Windows

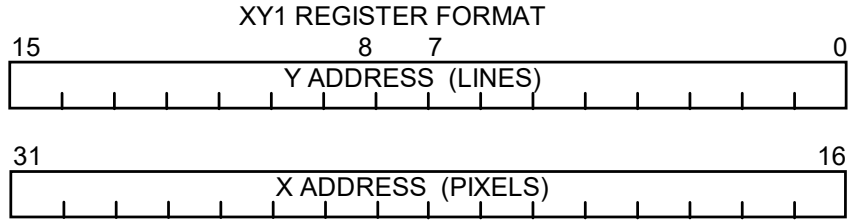
There are three XY registers that are utilized during read or write transfers: XY0, XY1, and XY2. XY0 defines the offset into the first host word of every line that is to be read or written. The XY0 format is shown below:



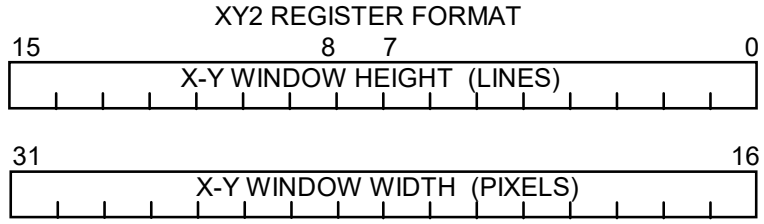
In 8, 16, or 32 bit/pixel mode, the offset specifies where within **the first data dword** of a line the first valid byte of data occurs. Allowable values for offset are 0 to 3., however, the offset should normally be set to the first pixel of data within a dword. This implies that in 32 bit/pixel mode that the offset be set to 0. In 16 bit/pixel mode, the offset should be either 0 or 2. In 8 bit/pixel mode, the offset can be 0 to 3.

If the offset is set to 0, the first data dword contains four bytes of valid data. If the offset is set to 1, the lowest byte of the first data dword is ignored. If the offset were set to 3, the lower three bytes of the first data dword would be ignored. The offset applies to only the first dword of data transfers. Subsequent transfers within a line assume that the entire 32 bit word is valid. In 1 bit/pixel mode (stipple mode), offset specifies where within the first data word the first valid bit of data occurs. Allowable values for offset are from 0 to 31.

The XY1 register specifies the starting address of the X-Y window in local memory space in terms of X-Y coordinates. The X-Y address is combined with the linear origin address in DE_ORG to compute the absolute linear address. XY1 should be programmed after all other XY and drawing parameter registers since writing XY1 will trigger the transfer command. The XY1 format is shown below:



The XY2 register specifies the width and height of the X-Y window in terms of pixels and lines respectively. The XY2 register format is shown below:



A.3.2 Drawing Parameter Registers for X-Y Windows

Since an XY window transfers data through the drawing pipeline, all applicable drawing parameter registers must be programmed appropriately. During a read transfer, the following drawing parameter registers must be programmed:

BUF_CTRL	Buffer Control Register
XYW_AD	XY Window Address
XYW_SZ	XY Window Size
DE_PGE	Page offset into local buffer(s)
DE_SORG	Origin of read data
DE_SPTCH	Source data pitch
CMD_OPC	Opcode for RXFER (0x6)

During a write transfer, the host data is treated as source data and the following drawing parameter registers must be programmed:

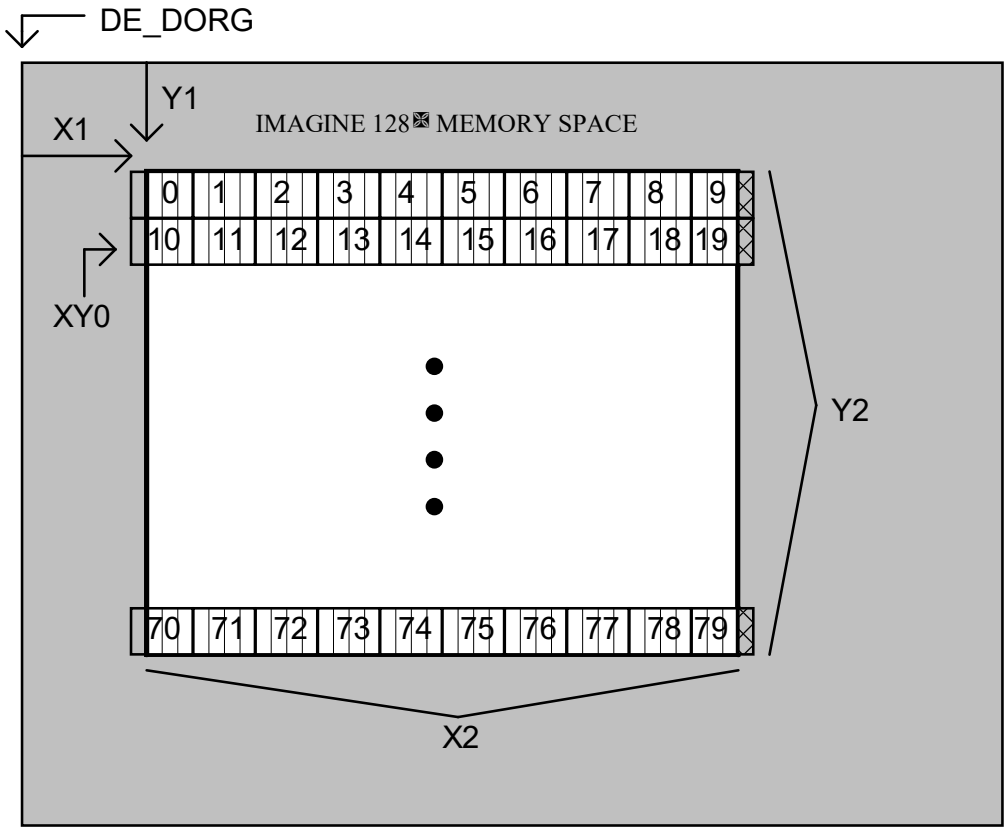
BUF_CTRL	Buffer Control Register
XYW_AD	XY Window Address
XYW_SZ	XY Window Size
DE_PGE	Page offset into local buffer(s)
DE_DORG	Origin of destination data
DE_DPTCH	Destination data pitch
CMD_OPC	Opcode for WXFER (0x7)
CMD_ROP	Raster operation
CMD_STYLE	Command Style
CMD_CLP	Clipping Control
FORE	Foreground Color Register
BACK	Background Color Register
MASK	Plane Mask
RMSK	Raster Mask
CLPTL	Top Left Clip
CLPBR	Bottom Right Clip

A.3.3 XY Window Example

The diagram below illustrates a XY window for a write transfer. The starting address of the window is specified by DE_DORG offset by X1 pixels and Y1 lines. The width of the window is X2 pixels and the height is Y2 lines. In this example, X2 is programmed for 38 pixels and Y2 is programmed for 8 lines. The first word offset, XY0, is programmed to 1 pixel. The pixel depth is assumed to be 8 bits/pixel.

The first 32 bit word of data that the host transfers through the XY window, word 0, will be written to the first location of the XY window. Since XY0 is set to 1, the first pixel of the first word is discarded. Therefore, only three pixels from the first host word are written. The next eight host data words are written in their entirety to consecutive locations. At this point, a total of 35 pixels have been written: 3 from the first word and 32 from the next eight words. Since the window was programmed to 38 pixels wide, only three pixels from word 9 will be written. It is very important to realize that the last pixel of word 9 will be discarded. It cannot contain the first pixel of data for the next line. It is software's responsibility to make sure that bitmaps that are transferred through an XY window are padded appropriately.

Word 10 of host data will be written to the first location of the second line with the first pixel discarded due to XY0 being set to 1. Host data will continue to be written in the manner described above until the last pixel of the last line is written. When the last pixel is written, the transfer is considered complete and any additional data written to the window will be ignored. Data from the host is always considered to be sequential. Any time data is not sequential, a new XY1 value must be loaded corresponding to the new address of the data.



A.4 Control of the Command Pipeline

Control of the command pipeline is a three step process.

Step 1. Ensure that IMAGINE 128™ is ready to accept new data.

Step 2. Update registers.

Step 3. Trigger New command.

IMAGINE 128™ employs extensive pipelining to smooth the process of loading new commands and parameters. When a command begins execution, all of the required parameters are transferred from the host accessible registers to internal working registers. When the parameters have been transferred to internal registers, IMAGINE 128™ is ready to accept a new command and parameters into its host accessible registers.

The command is queued for execution once the command trigger register (XY1) or the 3D_TRIG register (for 3D lines and triangles) has been written. This register must be the last one written in any command sequence. It is important to note that a command will not be triggered unless the most significant byte of XY1 or 3D_TRIG has been written. As soon as the trigger is written, IMAGINE 128™ will acknowledge by asserting the BUSY signal. A command that is ready for execution must still wait for a previous command to complete execution before it will actually start. During this waiting period, BUSY will remain set.

There are four additional bits that may be monitored to control the command pipeline. PRV (FLOW[3]) has two separate interpretations. During a write transfer, PRV=1 implies that at least half of the data cache is ready to receive data. During all other operations, PRV=1 indicates that the previously triggered command is still executing. It is similar to BUSY, except that PRV will not be de-asserted until both the drawing engine and memory controller have completed all operations associated with the previously triggered command. PRV is useful when operating the drawing engine in "dual cache mode".

CLP (FLOW[2]) will indicate that the command that just completed did so as the result of a clipping condition (i.e. stop on clip boundary). The CLP bit is cleared every time a new command begins execution, so it is important not to pipeline commands if the status of CLP is to be relied on.

Drawing Engine Busy (DEB- FLOW[0]) and Memory Controller Busy (MCB - FLOW[1]) provide additional visibility into the internal state of IMAGINE 128™. The drawing engine is idle when no commands are currently in execution. The memory controller will assert MCB when it is currently running a memory cycle or has a request for a memory cycle in its queue. Note that refresh or display transfer cycles alone will not cause MCB to be asserted, however they will cause MCB to be held if there are normal memory requests in the memory controller queue. The MCB bit is very useful in determining the integrity of data to be read back from the local buffers.

Control of the Command Pipeline (Continued)

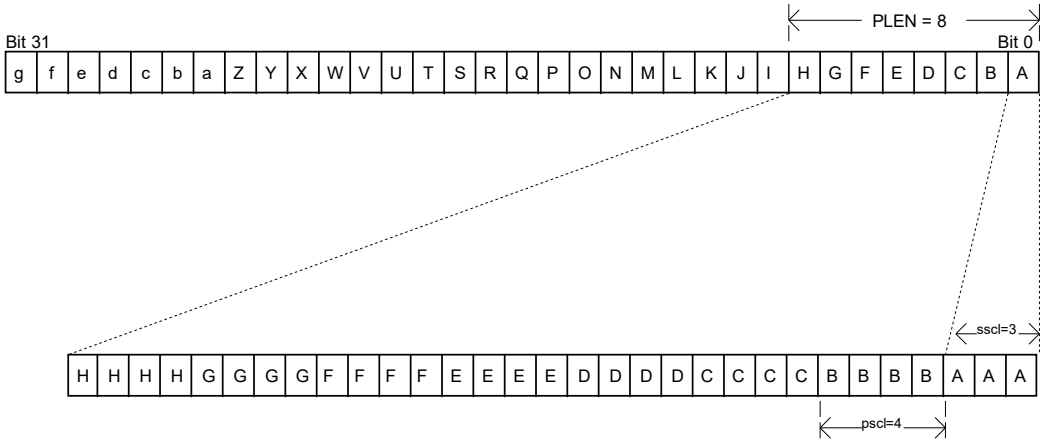
When utilizing X-Y windows, the pipe line must be controlled in a slightly different way. As with any command, the BUSY signal must be monitored before any new parameters are loaded into the host accessible registers. After setting up the X-Y transfer, the DEB bit must be checked to insure that the drawing engine has completed its current command. When the drawing engine is idle, the X-Y transfer may be triggered. When all X-Y data has been transferred from the host, the DEB should again be checked to ensure that the drawing engine is idle before the next command can be triggered. If this is not done, it is possible that there still could be valid data in the cache that could be corrupted if another command it triggered. It is important to note that DEB will remain active until all the data specified by the X-Y parameters has been transferred.

A.5 Draw Style and Patterning

Line Style	SOLID	TRNSP	LPAT bit	Result
Line solid	1	X	X	Foreground
Line on off dash	0	1	0	Destination
Line on off dash	0	1	1	Foreground
Line double dash	0	0	0	Background
Line double dash	0	0	1	Foreground

The LPAT bit is the corresponding bit in the pattern register. In addition, the dash members may be controlled by the settings in the pattern register (LPAT) and the pattern control register (PCTRL). The LPAT register is a simple 32 bit stipple pattern that selects foreground, background or transparent depending whether each bit is set or cleared and the state of the TRNP bit. PCTRL allows for scaling and cropping of the LPAT bit pattern.

The scaling factor is specified in the PSCL register and will cause each bit in the pattern register to be scaled from one to eight times. The SSCL register specifies the scale to be applied to the first bit in the pattern this value must be less than PSCL. The PLEN register specifies the pattern length, starting with LPAT[0]. Note that PLEN specifies pattern bits and not pixels drawn. For example, if PLEN is 10 (decimal) and PSCL is 5 (decimal) the total number of pixels drawn would be 50 (decimal) with each of the 10 pattern bits replicated 5 times.



The PATRN register provides additional information as to how to start and end. The NLST (no last) bit will cause the line algorithm not to draw the last pixel in the line, and not increment the line pattern for that pixel. This should be used in the drawing of poly lines where the end point of one line segment is common with the start point of the next line segment.

The PRST (pattern reset) bit will cause IMAGINE 128 to initialize the pattern at the start of each new LINE command. If PRST is not set, the pattern will be continuous from line to line.

For BITBLT and TRIAN, the APAT bit in the PATRN register will cause the source to be a 32x32 tile of pixels or stipple pattern if stipple is set. This pattern is locked to the screen, that is to say two abutting triangles or rectangles will have matching patterns at their edges.

A.6 Fill Style and Patterning

Fill Style	SOLID	TRNSP	STPL	stipple bit	Result
Fill Solid	1	X	X	n/a	fore op dst
Fill Tiled	0	0	0	n/a	src op dst
Fill Stippled	0	1	1	0	destination
Fill Stippled	0	1	1	1	fore op dst
Fill Opaque Stippled	0	0	1	0	back op dst
Fill Opaque Stippled	0	0	1	1	fore op dst

The transparency function is only meaningful when a stipple operation is being executed. Transparency should be set to zero at all other times.

A.7 Display List Processor

The Imagine 128 contains a Display List Processor (DLP) which can read drawing engine commands from memory and execute them. The DLP can accept four distinct formats, XY format (format 1), REG3 format (format 0), DMA format, or text mode. The format is selected when writing the end address, however a given format must be held constant though an entire list. Therefore list formats cannot change until after writing a new start address, or the list reaches an explicit stop point, and a new end address is written with the new format. It is very important that software maintain coherency by abiding by the above rules or the display list can have unpredictable results.

The XY Format is suitable for applications where only XY0 through 3 need to be accessed. The REG3 format provides the most flexibility where individual registers need to be accessed. The DMA format can start multiple DMA requests over AGP. Finally, the text mode provides a very efficient means of cacheing glyphs and drawing them rapidly to the screen.

Selecting format 0 specifies the Register/DMA mode. Setting bits 25:24 to 0 specifies the Non-DMA register format. Three registers can be specified by writing the lower 8 bits of the drawing engine registers into the first 3 bytes of the command. The upper 8th bit (or bank select) for each of the registers is located in bits 28-30 respectively. Bit 31 specifies waiting for vertical blank before executing the list. Bits 32 through 27 specify the register values to be written in the three registers, and bits 26-27 select the number of registers to be written (1-3). Registers are always written from A-C, no gaps allowed.

Setting bits 25:24 to a 01 selects the DMA mode. This mode may be used to request Multiple AGP DMA transfers. If bit 31 is set, then the DLP will wait after the current AGP request until it is complete.

Setting bit 25 to a 1 selects Text mode. In text mode, up to two glyphs can be specified, plus their destination addresses. The glyphs each have their own text table entry which provides information about the glyph to enahance rapid accessing. Software must set up all registers not accessed by the DMA, but needed for writing text, prior to executing this command. REG3 mode can be used to do this.

Any version of format 0 are allowed to be mixed within a single list.

After the data is ready for display list execution, the application must set the start and end addresses. The display list start address is loaded into DL_ADR. The display list end address is loaded into DL_CNTRL and the stop bit is set to 0. This triggers execution of the list. Three other bits are used for display list control. DL_SEN selects the primary or virtual buffer, DL_FMT selects the format, and DL_SVD selects DMA mode. These three buffers must follow the following rules to maintain coherency:

1) They can never be changed while a list is executing.
2) They can only be changed after a start address is written (for the new list), or only after a list has become idle and a new end address is written.

The DLP maintains two independent lists, an active list and pending list. The active list is the currently running list which is triggered by a start address and end address pair. It is possible to append to the list by writing to just the end address. This allows dynamic list building.

Whenever a list is running, a new start address can be written which will change the internal pointer to the pending list. The old list will continue executing, but all subsequent end addresses will now be associated with the pending lists start address. The pending list can be treated just like the primary list.

If a third start address is written, retries will be issued until the pending list becomes the active list and there is room for a new pending list.

** NOTE: The stop bit will stop all lists, including any pending lists and cause the lists to be inaccessible.

A.8 Texel Cache

The Imagine 128 is equipped with an advanced 8KB texel cache (TC) which greatly improves texture mapping and video applications. The cache can handle several palette and non-palette texture formats with sizes up to 512x512. Mipmapping is supported up to 10 levels of detail. The TC is capable of generating 4 texels/clock for 1 clock cycle bi-linear interpolation. It also employs an advanced look ahead algorithm for minimizing memory reads.

A.8.1 TC Sizes

The texture cache is capable of handling textures (or video frames) of up to 512 x 512 with the following restrictions. Textures must be a power of 2 in both X and Y directions. X and Y sizes are independent, i.e. 2 x 64, 128 x 32, etc.. are allowed.

The cache is optimized for an efficient use of space, however the following formats (or smaller) work best as they will fit directly into the cache:

Texture Format (bits per textured pixel (bpt))	Texture Size (XxY)
32 bpt	32x64
16 bpt	64x64
8 bpt (palettized or direct)	128x64
4 bpt (palette)	256x64
2 bpt (palette)	512x64
1 bpt (palette)	512x64

Using textures of the above size or less will result in the maximum number of hits, minimizing misses and greatly improving cache performance.

A.8.2 Texture Formats

Please see the register definition section for TEX_CTRL

A.8.3 Special Commands

Their are two commands associated with the texture cache, INV_TEX and LD_PAL. The INV_TEX command Instructs the texel cache that the next triangle coming through is using a different texture than the previous ones.

The LD_PAL command must be used prior to a palettized texture map if the palette hasn't been loaded. This command will load a palette for use.

A.9 Blending

The Imagine 128 implements full OpenGL compatible alpha blending. The blending function can be applied to any Drawing Engine command. The Control of blending is performed in the ACNTRL register.

To properly set up a blending command, the following must be done. First, select a source and destination blending function. These are defined in the lower byte of the ACNTRL register. Second, if you are in a mode which doesn't support alpha or are going to use the source or destination alpha registers, you must load them into the lower two bytes of the ALPHA register. If you are in a mode which supports alpha and you want to use the constant registers, you must set the SRE and DRE bits to override the default settings. Finally, the blending enable bit must be set to activate blending.

A.10 Programming Imagine 128^3, 3D Operations

The Imagine 128 is a vertex-based 3D polygon accelerator. It performs the setup for 3D triangles, lines and points in hardware.

NOTE: The one exception is that setup needs to be done for 32 bit Z.

A.10.1 Mechanism

There are 2 3D commands:

1) TRIAN_3D
2) LINE_3D

NOTE: LINE_3D can be used to render 3D points.
NOTE: Texture Mapped 3D Lines are not supported.

There are up to three steps to take to specifically program for a 3D operation:

Step 1: Control and Mode Setup
Step 2: Parameter Load
Step 3: Trigger

Step 1: Control and Mode Setup

a)	BUF_CTRL:	<27:26>	Source Pixel Size and Format
		<25:24>	Destination Pixel Size and Format
b)	DE_SORG:		Source Origin
c)	DE_DORG:		Destination Origin
d)	DE_ZORG:		Z-Buffer Origin
e)	DE_SPTCH:		Source Pitch
f)	DE_DPTCH:		Destination Pitch
g)	DE_ZPTCH:		Z Pitch
h)	CMD:		Command
i)	FORE:		Foreground Color
j)	BACK:		Background Color
k)	MASK:	0xFFFFFFFF	Pixel Plane Mask
l)	LPAT:		Line Pattern (For 3D Lines)
m)	PCTRL:		Line Pattern Control (For 3D Lines)

The following origins apply to texture mapping mode:

n)	LOD0_ORG:	Texture Mipmap Level 0 Origin
o)	LOD1_ORG:	Texture Mipmap Level 1 Origin
p)	LOD2_ORG:	Texture Mipmap Level 2 Origin
q)	LOD3_ORG:	Texture Mipmap Level 3 Origin
r)	LOD4_ORG:	Texture Mipmap Level 4 Origin
s)	HITH:	Hither Value (For Z-Buffer Enabled)
t)	YON:	YON Value (For Z-Buffer Enabled)
u)	FOG_COL:	Fog Color (For Fog Mode)
v)	ALPHA: <23:16>	Alpha Test Value (For Alpha Compare)
w)	A_CNTRL:	Alpha Control Register
x)	C3D_CNTRL:	3D Control Register
y)	TEX_CNTRL:	Texture Map Control Register

Step 2: Parameter Load:

a) CP0: Pattern Pointer
b) CP1: Vertex 0 X
c) CP2: Vertex 0 Y
d) CP3: Vertex 0 Z
e) CP4: Vertex 0 W
f) CP5: Vertex 0 Color {A,R,G,B}
g) CP6: Vertex 0 Specular {F,Rs,Gs,Bs}
h) CP7: Vertex 0 U
i) CP8: Vertex 0 V
j) CP9: Vertex 1 X
k) CP10: Vertex 1 Y
l) CP11: Vertex 1 Z
m) CP12: Vertex 1 W
n) CP13: Vertex 1 Color {A,R,G,B}
o) CP14: Vertex 1 Specular {F,Rs,Gs,Bs}
p) CP15: Vertex 1 U
q) CP16: Vertex 1 V
r) CP17: Vertex 2 X
s) CP18: Vertex 2 Y
t) CP19: Vertex 2 Z
u) CP20: Vertex 2 W
v) CP21: Vertex 2 Color {A,R,G,B}
w) CP22: Vertex 2 Specular {F,Rs,Gs,Bs}
x) CP23: Vertex 2 U
y) CP24: Vertex 2 V

Note: **The next 6 parameter registers only need to be loaded in 32 Bit Z mode. If not in 32 Bit Z mode, these 6 parameters must not be loaded; otherwise, unpredictable results would occur.**

z) CP25: Low 32 Bit Z at SPXY
aa) CP26: High 12 Bit Z at SPXY
bb) CP27: Low Change in Z with respect to X
cc) CP28: High Change in Z with respect to X
dd) CP29: Low Change in Z with respect to start edge
ee) CP30: High Change in Z with respect to end edge

Note: **The three sets of parameters (CP1-CP8), (CP9-CP16) and (CP17-CP24) represent the parameters for the three vertices of a 3D triangle. For the 3D Line or Point, (CP9-CP16) and (CP17-CP24) represent the parameters for the two endpoints. Since texture mapped lines are not supported, the (w,u,v) parameters for 3D Line or Point commands are meaningless.**

Step 3: Trigger

Writing into 3D_Trigger Register will trigger the 3D command. This register needs only to be written to, no data need be supplied, and no data is contained within.

A.11 3D Operational Modes and Control

For 3D triangle commands, the minimal set of CP parameters you need to set are the x,y coordinate pairs for the three vertices (CP1, CP2), (CP9, CP10), and (CP17, CP18). For 3D line commands, the minimal set of CP parameters you need to set are the x,y coordinate pairs for the two endpoints (CP9, CP10), and (CP17, CP18).

A.11.1 Gouraud Shading Mode

- To enable Gouraud Shading, set ***C3D_CNTRL<24>*** = 1.
- Must disable SOLID mode by setting ***CMD<16>*** = 0.
- Set the color values for the three vertices of the triangle (CP5, CP13, CP21).

-OR- set the color values for the two endpoints of the line (CP13, CP21).

A.11.2 Specular Highlighting Mode

- To enable Specular Highlighting, set ***C3D_CNTRL<25>*** = 1.
- Set the Specular color values for the three vertices of the triangle (CP6, CP14, CP22).
  -OR- set the Specular color values for the two endpoints of the line (CP14, CP22).

A.11.3 Z Buffer Mode

- To enable Z-Buffering, set ***C3D_CNTRL<0>*** = 1. If disabled, no z-buffer hidden surface removal or z-buffer updates would occur.
- Disable Read Only Z (***C3D_CNTRL<1>*** = 0) if Z compares and Z-Buffer updating are desired. If Enabled, Z compares would occur, but the Z-Buffer would not be updated..
- Usage of Perspective Z and Low Resolution Z (***C3D_CNTRL<3:2>,*** respectively) is summarized in the following table:

Pixel Size	Low Resolution Z	Orthogonal Z	Clamping	Setup	Z Size	Dest Zsize
8bpp	N/A	N/A	*N/A*	N/A	N/A	N/A
16bpp	N/A	Yes	*16bpp*	Yes	16bpp	16bpp
16bpp	N/A	No	*24bpp*	Yes	16bpp	16bpp
32bpp	Yes	Yes	*24bpp*	Yes	24bpp	32bpp
32bpp	Yes	No	*24bpp*	Yes	16bpp	32bpp
32bpp	No	N/A	*32bpp*	No	32bpp	32bpp

- Z Compare Operators: (***C3D_CNTRL<7:5>***) See 5.8.35 for the table of Z compare operators used in Z-Buffer hidden surface removal operation.
- **Note:** If Z Compare Operator is set to ALWAYS (***C3D_CNTRL<7:5>*** = 0x1), performance will be enhanced by 40%. An example of an application that would utilize this performance enhancing feature would be Z Fills.
- Yon Compare Operators: (***C3D_CNTRL<10:8>***) See 5.8.35 for the table of Yon compare operators used in Yon Z Clipping surface removal operation.
- Hither Compare Operators: (***C3D_CNTRL<13:11>***) See 5.8.35 for the table of Hither compare operators used in Hither Z Clipping surface removal operation.
- If *not* in 32-bit Z mode, set the z values for the three vertices of the triangle (CP3, CP11, CP19)

-OR- set the z values for the two endpoints of the line (CP11, CP19).

- If in 32-bit Z mode, the start Z (CP25, CP26), Delta Z/Delta X (CP27, CP28), and Gradient Z values (CP29, CP30) must be set for the 3D triangle, line and point commands.

A.11.4 Fog Mode (vertex) (C3D_CNTRL[4] = 0)

- To enable Fog, set ***C3D_CNTRL<27>*** = 1. When fog is enabled, you have the option to enable fogging (***C3D_CNTRL<26>*** = 1) onto the alpha value.
- Set the (1-fog) percentage value (with respect to the fog color specified in the FOG_COL register) for the three vertices of the triangle (CP6, CP14, CP22) -OR- set the (1-fog) percentage value for the two endpoints of the line (CP14, CP22).

A.11.4 Fog Mode (Fog Tables) (C3D_CNTRL[4] = 1)

- Fog tables are loaded via the host bus by setting the CS bit in BUF_CNTRL before writing to the Silverhammer cache. There are 65 entries in the table. Fog Tables use 1/w to index into them, where 1/w is approx. 0, is the first entryl. When 1/w is 2, then we are pointing at the 64th entry.

A.11.5 Alpha Modes and Control

A.11.5.1 Alpha Comparison

- To enable Pixel Alpha Compare, set ***A_CNTRL<19>*** = 1.
- Set the Alpha Test Value in ***ALPHA_REG<23:16>***.
- The Pixel Alpha Compare Operators are set in ***A_CNTRL<18:16>***. See 5.8.35 for the table of alpha compare operators used in Alpha Clipping.
- If the alpha value to be compared is originating from the vertices of the triangle or line, set the alpha values for the three vertices of the triangle (CP5, CP13, CP21)

-OR- set the alpha values for the two endpoints of the line (CP13, CP21).

A.11.5.2 Alpha Select and Modulation

- Pixel Alpha Select (***A_CNTRL<24>***) will select alpha value from current texel if A_CNTRL<24> is set to 0 and texture mode (***TEX_CNTRL<0>*** = 1) is enabled. Otherwise, the alpha value will be selected from either the interpolated pixel value, foreground or background value, i.e. non_texel_alpha depending upon which pixel color mode is set.
- Enable Alpha Modulation (***A_CNTRL<25>*** = 1) will, with texture mode enabled, modulate the texel alpha value with non_texel_alpha.

Note: If Alpha Select and Alpha Modulation are both set, the alpha value would be set to zero.

Texture Mode	Alpha Select	Alpha Modulation	Alpha Value
0	0	0	*Gourard Shaded, Flat Shaded, or Bg/Fg (Line) Alpha*
0	0	1	*Gourard Shaded, Flat Shaded, or Bg/Fg (Line) Alpha*
0	1	0	*Gourard Shaded, Flat Shaded, or Bg/Fg (Line) Alpha*
0	1	1	*ZERO*
1	0	0	*Texel Alpha*
1	0	1	*Alpha Modulated Texel Alpha*
1	1	0	*Gourard Shaded, Flat Shaded, or Bg/Fg (Line) Alpha*
1	1	1	*ZERO*

A.11.5.3 Decal Alpha Mode

- Enabling Decal Alpha Mode (***A_CNTRL<26>*** = 1) would perform the following alpha blending function:

RGB = (Texel_RGB)*(Texel_Alpha) + (Non_Texel_RGB)*(1-Texel_Alpha).

A.11.6 Texture Map Modes and Control

A.11.6.1 Texture Map

- To enable Texture Map Mode, set ***TEX_CNTRL<0>*** = 1.
- Set the perspective w values for the three vertices of the triangle (CP4, CP12, CP20).
- Set the u,v texel coordinate values for the three vertices of the triangle (CP7, CP8), (CP15, CP16) and (CP23, CP24).
- ***Important: Each vertex w must be written before its respective vertex u,v coordinate pairs.***
- **Disabling this mode disables the rest of the texture map related modes.**

A.11.6.2 MipMap Modes

- To enable MipMap Mode, set ***TEX_CNTRL<1>*** = 1.
- To enable MipMap Correction Mode, set ***TEX_CNTRL<2>*** = 1.
- Can set up to five MipMap Level-of-Detail Origins (LOD0_ORG, LOD1_ORG, LOD2_ORG, LOD3_ORG and LOD4_ORG, where LOD0_ORG is the origin of the largest texture mapped image.) where each level of mipmaps is one-half the size of the previous mipmap. When texture map mode is enabled, LOD0_ORG must be set, whether or not mipmapping is enabled or not.
- Trilinear Mipmapping is a two pass process. On the first pass, render the texture-mapped triangle. On the second pass, re-render the same triangle, but enable Trilinear Mipmapping Mode by setting ***TEX_CNTRL<3>*** = 1. This will give you trilinear mipmapping.
- Number of Mipmaps: (***TEX_CNTRL<15:13>***) Specifies the number of level of detail mipmap images to be used for texture mipmapping. Imagine 128^3 will support up to 5 level of detail mipmaps per texture image. Refer to the specification for the bit definition.
- Mipmap width and height of the largest level of detail mipmap texture image are to be specified in (***TEX_CNTRL<19:16>***) and (***TEX_CNTRL<23:20>***), respectively. Imagine 128^3 will support texture images up to a maximum size of 512x512. The width and height must be a power of 2 and they need not have to be equal, i.e. Imagine 128^3 supports square, as well as, rectangular texture images.

A.11.6.3 Texture Modes

- The Nearest Mode bit (***TEX_CNTRL<4>***) is a toggle bit between Nearest Mode and Bilinear Interpolation Mode. Setting the bit to 1 will enable Nearest Mode. Setting it to 0 will enable Bilinear Interpolation Mode.
- To enable RGB Modulation Mode, set ***TEX_CNTRL<5>*** = 1. This mode modulates the texture image with an interpolated rgb surface generated by the Gouraud shader. So, Gouraud Shading needs to be enabled by setting ***C3D_CNTRL<24>*** = 1 and the three color parameters (or two, depending upon the rendering command) need to be set (see Gouraud shading).
- To enable Perspective Correction, set ***TEX_CNTRL<6>*** = 1. The w parameters (CP4, CP12, CP20) need to be set to its appropriate perspective values.

A.11.6.4 Texture Map Mirror Modes

- Texture mirroring provides a convenient method for software to provide reflective environment texture mapping. This allows triangles to be drawn normally without concern for vertex flipping to match the orientation of the texture.
- There are four texture map mirroring modes:

TEX_CNTRL<11>	TEX_CNTRL<10>	Texture Map Mirror Mode
0	0	No Mirroring
0	1	Mirror with respect to x.
1	0	Mirror with respect to y.
1	1	Mirror with respect to x and y.

A.11.6.5 Texture Image Pixel Format

- Texture Image Pixel Format (***TEX_CNTRL<28:24>***). Imagine 128^3 support palletized and non-palletized texture image pixel formats. Refer to the specification for a list of supported formats and its corresponding encoding in TEX_CNTRL<28:24>.

A.11.7 Pixel Color Table

Non_Texel_Color Priority
1) Foreground Color if SOLID (***CMD<16>*** = 1) is enabled.
2) Background Color if internal pattern bit is set to zero.
3) Foreground Color if internal pattern bit is set to one and Gouraud Shading is not set.
4) Interpolated Gouraud Shaded Color if internal pattern bit is set to one and Gouraud Shading is set.

Texel_Color Priority (When texture mode (***TEX_CNTRL<0>*** = 1) is enabled.)
1) RGB Modulated Texel if RGB Modulation (***TEX_CNTRL<5>*** = 1) is enabled.
2) Decal Alpha Blended Texel if Decal Alpha Mode (***A_CNTRL<26>*** = 1) is enabled.
3) Texel Color.

Note: Texture Map Mode bit (***TEX_CNTRL<0>***) will select between the two possible Pixel Value. If texture map mode is enabled (***TEX_CNTRL<0>*** = 1), then the Texel Color is selected. Otherwise, the Non_Texel Color is selected.

A.11.8 OpenGL Compatibility

The following registers are used in the table to generate all of the OpenGL functions.

Control	Definition	Register Location
ABS	Alpha Blend Select	3D_CTRL[17]
TBS	Texture Blend Select	3D_CTRL[18]
RSEL	RGB Select	3D_CTRL[19]
RM	RGB Modulation	TEX_CNTRL[5]
ASL	Alpha Select	ACNTRL[24]
AMD	Alpha Modulation	ACNTRL[25]
DA	Decal Alpha Blend	ACNTRL[26]

The following table shows the OpenGL blend functions and how they can be obtained using the SilverHammer graphics processor.

Texture FMT	Fragment	Replace	Modulate	Decal	Blend
Alpha	RGB	RSEL = 1 RM = x DA = x TBS = x	RSEL = 1 RM = x DA = x TBS = x	Undefined	RSEL = 1 RM = x DA = x TBS = x
	A	ASL = 0 AMD = 0 ABS = 0	ASL = 0 AMD = 1 ABS = 0		ASL = 0 AMD = 1 ABS = 0
:Luminance	RGB	RSEL = 0 RM = 0 DA = 0 TBS = 0	RSEL = 0 RM = 1 DA = 0 TBS = 0	Undefined	RSEL = 0 RM = 0 DA = 0 TBS = 1
	A	ASL = 1	ASL = 1		ASL = 1
Luminance Alpha	RGB	RSEL = 0 RM = 0 DA = 0 TBS = 0	RSEL = 0 RM = 1 DA = 0 TBS = 0	Undefined	RSEL = 0 RM = 0 DA = 0 TBS = 1
	A	ASL = 0 AMD = 0 ABS = 0	ASL = 0 AMD = 1 ABS = 0		ASL = 0 AMD = 1 ABS = 0
Intensity	RGB	RSEL = 0 RM = 0 DA = 0 TBS = 0	RSEL = 0 RM = 1 DA = 0 TBS = 0	Undefined	RSEL = 0 RM = 0 DA = 0 TBS = 1
	A	ASL = 0 AMD = 0 ABS = 0	ASL = 0 AMD = 1 ABS = 0		ASL = 0 AMD = 0 ABS = x
RGB	RGB	RSEL = 0 RM = 0 DA = 0 TBS = 0	RSEL = 0 RM = 1 DA = 0 TBS = 0	RSEL = 0 RM = 0 DA = 0 TBS = 0	RSEL = 0 RM = 0 DA = 0 TBS = 1
	A	ASL = 1	ASL = 1	ASL = 1	ASL = 1
RGBA	RGB	RSEL = 0 RM = 0 DA = 0 TBS = 0	RSEL = 0 RM = 1 DA = 0 TBS = 0	RSEL = 0 RM = 0 DA = 1 TBS = 0	RSEL = 0 RM = 0 DA = 0 TBS = 1
	A	ASL = 0 AMD = 0 ABS = 0	ASL = 0 AMD = 1 ABS = 0	ASL = 1 AMD = x ABS = x	ASL = 0 AMD = 1 ABS = 0