Trident

CYBER9320™ Flat Panel Controller

Features

Highly Integrated Design
- Requires only one 256Kx16 DRAM for 1024x768-16 color SVGA solution
- Built-in LUT-DAC composed of 256x18 color look-up table
- Dual loop memory and video clock
- Two-chip solution (9320 and 256Kx16) for 512K display memory
- Supports Extended-Data-Out (EDO) Memory
- 208-pin PQFP package

Accelerated Graphics Functions
- Optimized graphic engine for: BitBLTs, line drawing, short stroke vectors, rectangle fills, and text transfer
- Hardware pop-up icon (64x64x2-bit)
- Internal hardware cursor (64x64x2-bit or 32x32x2-bit)

Advanced Power Management
- Independent control for video clock, memory clock and DAC
- All register contents are accessible through the system bus, providing mechanisms for 0 V suspend and hibernation
- Supports self-refresh and slow-refresh DRAM for minimum power consumption

Versatile Display Support
- High resolution TFT, SS-STN, and CRT, including 1280x1024-16, 1024x768-256, 800x600-64K, 800x600-256, 640x480-256, 640x480-64K, and 640x480-16M colors

- High resolution DS-STN, including 1024x768-16, 800x600-256, 640x480-64K, and 640x480-256 colors
- Simultaneous display

Flexible Display Memory Interface
- 8-bit interface to mono SS/DS-STN, 8/16-bit interface to color SS/DS-STN, and 9/12/18/24-bit or analog interface to color TFT panels

Advanced Image Control
- Supports Frame Rate Control and Spatial Dithering for flat panel
- Auto-contrast adjustment
- Auto-fill and centering for high resolution panel

NTSC/PAL Encoder Support
- Provides RGB, composite sync, and carrier clock for NTSC/PAL encoder

Advanced Multimedia Support
- Allows 8/16 bits of external RGB video data to be input and merged with internal data stream

Simple Bus Interface Support
- Flexible Bus Interface Unit for zero wait state 32-bit glueless connection to VESA Local Bus (VL Bus), ISA, or PCI Bus 2.0 with no additional TTL
- Supports VESA DDC, DPMS, and VAFC standards
- Two wire interface to EEPROM or VESA DDC
- Linear display memory addressing

Mixed Voltage Operation and Interface
- Independent V_{CC} for internal logic, host interface, memory interface, and display interface
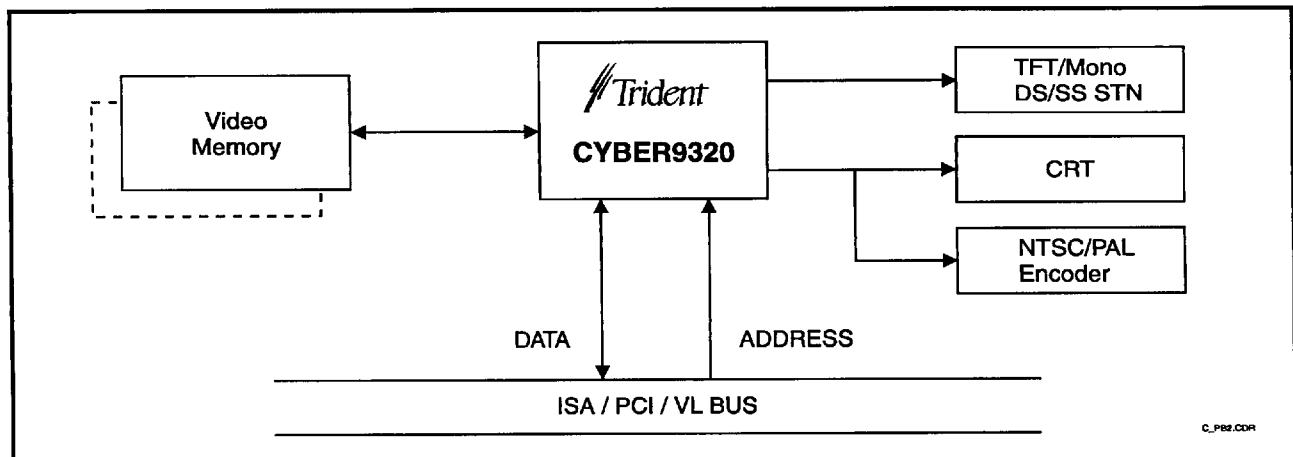
CYBER9320 Application Diagram

Overview

The CYBER9320 is a single-chip DRAM based, highly integrated graphic LCD/CRT controller for 32-bit VL Bus, PCI Bus, and ISA Bus interfaces. It provides a flexible, low cost, and high performance graphic solution for various color depths, CRT resolutions, panel resolutions, panel types, and display memory configurations. Offering zero-wait state local bus, efficient memory bandwidth, and a streamlined graphic engine, the CYBER9320 is an outstanding graphic accelerator for Microsoft Windows™, OS/2™, and other graphical user interfaces.

Highly Integrated Design

The CYBER9320's highly integrated design offers a "no TTL" solution for cost-effective, high performance graphic subsystem designs for the IBM™ PC and compatible notebooks. The integrated 24-bit TrueColor DAC and 108 MHz programmable clock synthesizer provide a complete graphic subsystem with the addition of only one DRAM. The CYBER9320 also includes a fully integrated GUI accelerator, read cache, and command FIFO that optimize memory bandwidth and maximize graphics performance. No TTL "glue logic" is needed for the system bus or display memory interface, and a two wire communications interface allows direct support of either an external EEPROM or VESA DDC monitor interface.

Accelerated Graphics Functions

The CYBER9320's graphics engine significantly boosts graphics performance through specialized hardware that accelerates the most frequently used GUI operations. Functions directly supported in hardware include: BitBLT, image and text transfer, line draw, short stroke vector draw, and rectangle fills. Graphic functions are optimized further by a hardware cursor (64x64x2 or 32x32x2 pixel image), which offloads the CPU for other data manipulation jobs. The hardware cursor mechanism can also be used to display patterns stored in the system memory. This pop-up icon is very useful in displaying user friendly information through simple hot key operations. The graphics engine also supports 256 Raster Operations (ROPs) for 8-bit per pixel (bpp), and 16 bpp graphic modes. These advanced functions allow significant performance increases over standard Super VGA designs, providing outstanding graphics acceleration in graphic intensive environments such as Microsoft Windows.

Advanced Power Management

The CYBER9320 provides flexible and extensive power management capabilities. The CYBER9320 supports 3.3V and 5V mixed voltage operation. The on-chip LUT-DAC, video clock (VCLK) and memory clock (MCLK) can be powered down through simple register controls. Power-down states includes ready, standby, suspend and hibernation. Each power state can be activated by hardware pins, hardware timers, or software control bits. All registers are accessible through the system bus. Register data can be saved and later on restored. The refresh clock can be turned off for further power savings with self-refresh DRAM. Slow-refresh DRAM is also supported in this design.

Versatile Display Support

The CYBER9320 features versatile display support in the following areas: flat panel, CRT, application display software drivers, and simultaneous display.

Flat Panel

The CYBER9320 supports TFT, Dual-Scan STN (DS-STN), Single-Scan STN (SS-STN), monochrome, and plasma panels without external glue logic. No extra frame buffers are required for DS-STN LCD's. Resolutions up to 1280x1024-16 Mono, STN, and TFT are supported. Resolution up to 1024x768-16 DS-STN is also supported.

CRT

The CYBER9320 display enhancements dramatically improve CRT resolution, providing sharp, HiColor images. These enhancements include support of non-interlaced 1280x1024-16, 1024x768-256, 1024x768-64K, 800x600-64K, or 640x480-16M colors for "full spectrum" color. Extended text modes of 80 or 132 columns by 25, 30, 43, or 60 rows provide an extended graphics area frequently used in many spreadsheet and database applications. In addition, extended graphics and text modes are supported by software drivers that provide a "ready-to-go" solution, minimizing the need for additional driver development.

Application Software Display Drivers

The CYBER9320 software drivers support the following applications:

Microsoft Windows	Ventura Publisher™
Wordstar™	Microsoft NT™
Autoshade™	CADKEY™
OS/2	Lotus™
FrameMaker™	AutoCAD™

P-CAD™   Quattro-Pro™

Microsoft Word™   VersaCAD™

Symphony™   WordPerfect™

SCO X-Windows™   Chicago™

The CYBER9320 also supports other VGA compatible applications using their respective software application drivers.

Simultaneous Display

The CYBER9320 displays data with up to 256 colors of 640x480 resolution on flat panel and CRT displays. This feature provides an optimal solution for users requiring data on both displays.

Flexible Display Memory Interface

The CYBER9320 offers display memory configurations from 1/2 MB to 1 MB DRAM configurations. A 32-bit memory bus interface and programmable DRAM timing provide a flexible interface that maximizes timing for increased performance. Additionally, a nominal DRAM interface requirement of one 256Kx16 DRAM for 1024x768-16 color SVGA minimizes chip count, system cost, and board space for a cost-effective design solution. The display memory interface also supports symmetrical or asymmetrical configuration and Dual CAS or Dual WE (Write Enable) DRAM configurations. Extended-Data-Out (EDO) DRAM is also supported to further enhance interface capabilities.

Advanced Image Control

Through advanced Frame Rate Control (FRC) and Spatial Dithering algorithm, color depths as high as 16M, 64K, or 256K are achievable for color flat panels. A 64-level gray-scale panel is also supported. Monochrome display quality for color applications is dramatically improved through autocontrast adjustment and advanced RGB color mapping methods. To enhance the image on high resolution displays, texts and graphics are expanded to fill the whole panel. In addition, the autocentering function relocates the display image to the center of the screen for the same purpose.

NTSC/PAL Encoder Support

RGB signals driven from the CYBER9320 LUT-DAC can directly interface with a standard off-the-shelf NTSC/PAL encoder. Composite synchronization signals also produced support the encoder for standard home TV connection.

Advanced Multimedia Support

A built-in VESA Advanced Feature Connector (VAFC) Port interfaces with the CYBER9320's 16-bit DAC to support high-speed and high-bandwidth video overlay on graphics or graphics output to video. This feature reduces the footprint for video subsystem design and provides a very economical solution for combining video and graphics in the same system. The CYBER9320 also supports palette snooping, which is ideal for multimedia applications.

Simple Bus Interface Support

A flexible Bus Interface Unit (BIU) provides a low cost, single chip solution for IBM PC or compatibles on VL Bus, PCI Bus, and ISA Bus systems. The CYBER9320's BIU supports a 16-bit ISA Bus interface and 32-bit VESA Local Bus (VL Bus) or PCI Bus interfaces. Combined with "glueless" connections, the BIU allows an efficient design path for quick and easy integration to future generation notebooks. The CYBER9320 supports VL Bus 2.0 speeds up to 50 MHz, PCI Bus 2.0 bus speeds up to 33 MHz, and ISA Bus speeds up to 12 MHz. Additionally, linear display memory addressing, zero-wait state host write buffer, read cache, and memory mapped I/O in PCI applications increase operating speeds and contribute to peak performance levels. Graphics system throughput is further enhanced by a command FIFO, allowing maximum bus transfer speed for applications such as Windows or AutoCAD that directly access video memory.

CRT Power Management

The CYBER9320 provides special CRT power management hardware features. The CYBER9320 supports four states of VESA Display Power Management Signaling (DPMS), which decreases monitor power consumption after a predetermined timeout period. VESA DPMS power-down states (ready, standby, suspend, and off) specify HSYNC and VSYNC signals to control the monitor power-down state.

Improved Manufacturability

The CYBER9320 is designed for high volume PC markets where the lowest possible manufacturing costs are required. To help achieve this, an internal Signature Analysis Circuit with built-in accumulator and timing circuit provides easy testing of both the integrity of the frame-buffer and the CYBER9320 functional circuitry. No external circuitry is required to support this feature.

Linear Addressing and Virtual Screen

A linear address memory interface improves system performance and allows larger images than the actual display size to be stored in the memory. "Display windows" inside the image are selected through a keyboard or a pointing device.

Complete Hardware Compatibility

The CYBER9320 is fully compliant with the PCI rev 2 and the VL Bus 2.0 specifications and supports VESA DDC and VAFC standards. The CYBER9320 is also 100% IBM VGA compatible on BIOS, register, and hardware levels, allowing full compatibility with virtually any VGA application software. Additionally, the CYBER9320 features a 208-pin PQFP package with optimized pin assignment for efficient PCB layout.
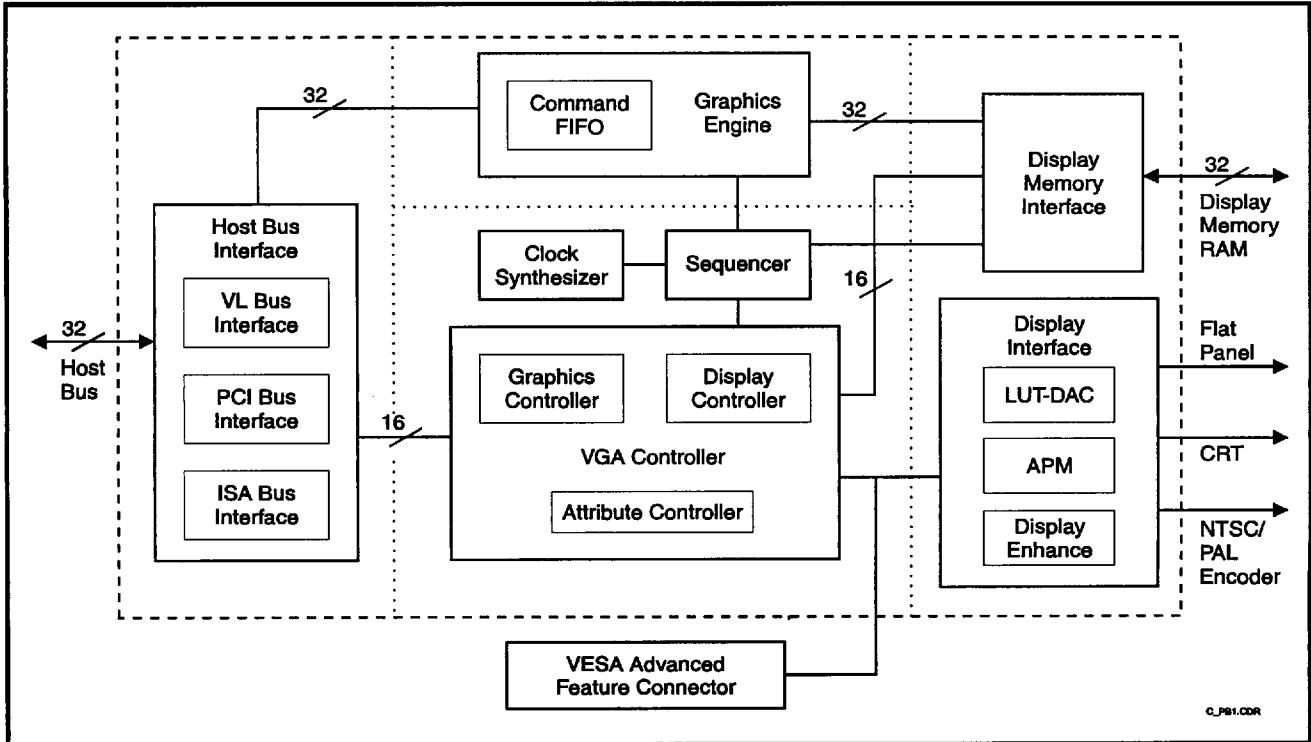
CYBER9320 Block Diagram

Contact your local Trident representative for:

- Data Sheets
- Technical Reference Manuals
- Evaluation Kits: Includes documentation plus evaluation board and software
- Reference Design Kits: Includes full documentation and software license for drivers to immediately enter production

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