Mobility M6
Pinout Specifications

Technical Reference Manual

The information contained in this manual has been carefully checked and is believed to be entirely reliable. No responsibility is assumed for inaccuracies. ATI reserves the right to make changes at any time to improve design and supply the best product possible.

Record of Revisions

Version	Date
First Draft	Jun 2000

Table of Contents

Chapter 1
Features Overview

1.1 Introducing M6

Maximum 2D & 3D Performance

M6 provides the fastest available 2D, 3D, and multimedia graphics performance for today's applications in full 32-bit color. Its 3D architecture also includes unprecedented innovations that enable advanced new features in upcoming applications, without compromising performance. With flexible memory support, M6 permits implementations targeted at both gaming enthusiast and workstation platforms.

Charisma Engine™

M6's Charisma Engine™ is the world's fastest geometry processing unit and is also the first to incorporate acceleration for advanced character animation features, including 4-matrix skinning and keyframe animation. These effects are critical for enabling game characters to display life-like facial expressions and to achieve fluid movement and motion.

Pixel Tapestry™ Architecture

M6 delivers the fastest 32-bit color rendering performance available, and supports three-way multitexturing and new 3D effects without compromising speed. The Pixel Tapestry™ Architecture is the first to be able to process up to 3 textures per pixel in a single clock cycle, bringing 3D worlds to life with incredible detail and realism. It easily deals with complex elements such as metals, liquids and wood and their interactions with lights and shadows.

Comprehensive Digital Video Support

M6 integrates industry leading digital video features, including advanced deinterlacing algorithms for unprecedented video quality and integrated digital TV decode capability. Combined with a tuner and demodulator, M6 provides an all-format DTV/HDTV solution, even including the 1920 pixel wide 1080i format. Coupled with the RAGE THEATER analog encoder/decoder chip, M6 provides a complete convergence solution.

Ideal for Windows 2000

M6 provides comprehensive support for all new Windows 2000 display-oriented features,

including acceleration of new GDI extensions like Alpha BLTs, Transparent BLTs, and Gradient Fills, as well as exclusive, patent-pending hardware alpha cursor support.

Flexible, High Performance Memory Support

M6 incorporates support for single or double data rate SDRAM/SGRAM at up to 200MHz, giving memory bandwidth of up to 6.4GB/s. Since memory bandwidth is increasingly becoming the largest barrier to performance in today's and tomorrow's most advanced applications, M6 features new HyperZ™ technology to boost effective memory bandwidth by over 20%.

1.2 General and Interfacing Features

- 32-bit PCI bus (Rev 2.2), 3.3 V with bus mastering support.
- Comprehensive AGP support including 3.3 Volt (AGP 2X) and 1.5 Volt (AGP 4X) mode operation, sideband addressing, AGP texturing (direct memory execution), and support for AGP reads and writes.
- Single channel 64-bit memory interface using SGRAM or SDRAM to build 8/16/32/64/128 MB configurations. Operating frequency is 125MHz minimum to 200MHz maximum, SDR or DDR. Gives memory bandwidth of up to 6.4GB/s.
- Support for ROM or Flash RAM parallel or serial video BIOS.
- Two independent CRT controllers to support two asynchronous simultaneous display paths.
- Integrated DAC for CRT with stereoscopic display support.
- Integrated second DAC for the second CRT support.
- Integrated TMDS transmitter running up to 165MHz for support up to 1600x1200 at 60Hz. Fully compliant with DVI and DFP connection standards.
- Support for external TMDS transmitter via 24-bit digital output to drive most popular TMDS transmitters up to 165MHz frequency
- Integrated dual channel LVDS interface up to 85MHz per channel. Supports up to QXGA resolution.
- Integrated enhanced TV encoder with 10-bit DAC (shared between second CRT DAC and TV)
- Independent DDC lines for both DACs and TMDS connections. Also full AppleSense support on DAC connection.
- External Spread Spectrum support for LVDS link to reduce EMI.

- Static and dynamic Power Management support (APM as well as ACPI) with full VESA DPMS and Energy Star compliance.
- Support for 8-bit and 16-bit video capture port including ZV port.
- Comprehensive testability including full internal scan, memory BIST, I/O xor tree and Iddq.
- Comprehensive 3D geometry acceleration capabilities, including transform, clipping, and lighting.
- Integrated geometry engine.
- Ideal accelerator for Windows 2000 - includes patent pending hardware support for the Windows 2000 alpha cursor, as well as acceleration of new GDI extensions such as Alpha BLTs, Transparent BLTs, and Gradient Fills.
- Integrated digital TV decode capability. Combined with a tuner an demodulator, M6 provides an all-format DTV/HDTV solution, including the 1920 pixel wide 1080i format.
- Fully compliant with expected PC 2001 requirements.
- Full ACPI 1.0b, OnNow, and IAPC (Instantly Available PC) power management, including PCI power management registers.
- Bi-endian support for compliance on a variety of processor platforms.
- Unique enhanced TCA (Triple-Cache Architecture) incorporates texture, pixel and vertex caches to maximize effective memory bandwidth.
- CCE high-speed pull architecture software interface optimized for Pentium III and Athlon systems:
    - Bus mastering of 2D&3D display lists.
    - Direct walk of Direct3D/OpenGL vertex list.
    - Ultra-thin driver layer.
    - Maximizes concurrency between RAGE 6 and host.
- Optimized for Pentium II SSE and AMD 3DNow! processor instructions.
- Triple 10-bit palette DAC supports pixel rates to 350MHz.
- DVI-compliant integrated 165MHz TMDS transmitter.
    - Up to UXGA (1600x1200) resolution.
    - Supports VESA proposed reduced blanking timings.
    - Ratiometric expansion.
- DDC1 and DDC2ci for plug and play monitors.

- Supports optional RAGE Theater companion chip for NTSC/PAL TV out and NTSC/PAL/SECAM analog video capture.
- Flexible memory support:
  - SGRAM or SDRAM.
  - SDR or DDR.
  - DDR support for both system memory SDRAM and graphics SGRAM devices.
  - 16MB to 128MB.
- High performance memory interface
  - 6.4GB/s with 200MHz DDR.
  - 3.2GB/s with 200MHz SDR.
  - Dual independent channels maximize memory efficiency.
- Integrated hardware diagnostic tests performed automatically upon initialization.
- High quality components through at-speed testing, built-in Scan, Iddq, CRC, chip diagnostics, and NAND tree.
- Single chip solution in 0.18 micron, 1.8V CMOS technology in 649 BGA package.
- Comprehensive HDKs, SDKs and utilities augmented by full engineering support.
- Complete local language support (contact ATI for current list).

1.3 Features in Details

1.3.1 2D Acceleration Features

- Highly-optimized 128-bit engine, capable of processing multiple pixels/clock. Higher speed compared to the RAGE 128 VR / GL chip due to various improvements.
- Hardware acceleration of Bitblt, Line Draw, Polygon / Rectangle Fill, Bit Masking, Monochrome Expansion, Panning/Scrolling, Scissoring, and full ROP support (including ROP3).
- Optimized handling of fonts and text using ATI proprietary techniques.
- Game acceleration including support for Microsoft's DirectDraw: Double Buffering, Virtual Sprites, Transparent Blit, and Masked Blit.
- Acceleration in 8/15/16/32 bpp modes.
- Significant increase in the High End Graphics WinBench score due to capability for C18 color expansion.

- Setup of 2D polygons and lines.
- Support for new WIN 2000 GDI extensions: Alpha BLT, Transparent BLT, Gradient Fill.
- Hardware cursor (up to 64x64x32bpp), with alpha channel for direct support of WIN 2000 alpha cursor

1.3.2 3D Acceleration Features

- Primitive (Triangle) set up rates of up to 20 Million triangles per second.
- 3D Texture support.
- Cubic Environment Mapping.
- Comphrehensive support for perturbation bump mapping (Tritech method): emboss, dot-product, and environment bump maps.
- Comprehensive enhanced 3D feature set:
  - Improved precision in Anisotropic filtering and Bilinear filtering.
  - Complete 3D primitive support: points, lines, triangles, lists, strips and quadrilaterals and BLTs with Z compare.
  - Improved texture compositing, with no limitations on texture formats or location (i.e., one texture may reside in AGP memory and the other in frame buffer memory).
  - Full screen or window double or triple buffering for smooth animation.
  - Support of special effects such as simultaneous alpha blending and fog (vertex and z-based), video textures, texture lighting, reflections, shadows, spotlights, LOD biasing and texture morphing. Filtered texture alpha channel, and hardware support for D3D ‘MODULATEALPHA’ texture blending mode.
  - Hidden surface removal using 16, 24, or 32-bit Z-buffering (maximum Z-buffer depth is 24 bits when stencil buffer enabled), 16 or 32-bit W-buffering.
  - 8-bit stencil buffer.
  - Line and Edge anti-aliasing.
  - 4 bits of subpixel and subtexel accuracy.
  - Gouraud and specular shaded polygons.
  - Advanced texture mapping support.
  - Perceptively correct per pixel mip-mapped texturing with LOD biasing and chroma-key support.

  - Support point sampled, bilinear, trilinear and anisotropic filtering.
  - Multi-texturing via three texture blending units, allowing 6 texel reads per pixel in a single tick and single pass. Allows effects such as: light and gloss maps, detail maps, reflections, shadows, spotlights, and texture morphing.
  - 3D Textures
  - Bilinear and trilinear texture filtering.
  - Full support of Direct3D texture lighting.
  - Dithering support in 16 bpp for near 24 bpp quality in less memory.
- Extensive 3D mode support:
  - Draw in RGBA32, RGBA16, & RGB16.
  - Texture map modes: RGBA32, RGBA16, RGB16, RGB8, ARGB4444, YC_rC_b444.
  - Compressed texture modes: YC_rC_b422, CLUT4 (CI4), CLUT8 (CI8), VQ, and DX6 mode.
- Full scene sort independent anti-aliasing.
- DX6 Color Compression.
- Improved support for DX6 Blend mode.
- Control bit for Vertex Walker zero area.
- Support for 32 bpp Palette (similar to the RAGE PRO LCD).
- Improvement to Chroma Key functionality (similar to the RAGE PRO LCD).
- Support for OpenGL format for Indirect Vertices in Vertex Walker.
- Support for DirectX 6.0 compressed texture scheme (i.e., color cell compression) that allows for higher benchmark scores.
- Hardware Z-buffer clear support.
- Maximum performance on AGP 4X platforms.
- Improved sub-textel accuracy to improve the appearance of highly magnified textures).
- Maximum performance of OpenGL on AGP 4X platforms.
- Improved performance in Raw Rendering and Geometry due to higher engine speed.
- On-chip texture cache dramatically improves large triangle performance
- On-chip vertical cache eliminates unnecessary vertex reads.

- HyperZ technology dramatically improves performance by maximizing Z-buffer efficiency.
- Optimized for full performance in true color triple buffered 32bpp acceleration modes.
- Second generation SuperScalar Rendering engine provides top 3D performance.
- Support for Microsoft's next generation GDI+ user interface:
  - Off axis 3D text readability improvement with anisotropic filtering.
  - Arbitrary texture sizes up to 2048x2048.

1.3.3 TCL (Transform, Clip, and Lighting) Features

- Dedicated geometry acceleration for Direct3D and OpenGL.
- HW Transformation, clipping and lighting rates of over 25 million triangles per second.
- Transforms homogeneous vertices from Object / Model Coordinates to Clip Coordinates
- Performs Frustum Clipping on the Point / Line and Triangle Primitives in Clip Coordinates
- Performs Texture Coordinate Transformation
- Supports DirectX skinning, with a 4-matrix / 2 vertex Vertex Blending (Skinning / Morphing (Tweening))
- View volume clipping and up to six user defined clip planes.
- Supports Guard-Band Clipping for clipping performance optimization
- Supports DirectX / OpenGL Texture Coordinate Generation
- Supports 6 User-Defined Clip Planes. Performance Optimizations Based on Coordinate Systems
- Supports OpenGL / DirectX Directional (Infinite) Lighting with Infinite & Local Viewer. Up to 8 Lights. Includes DX7 color-per-vertex support.
- Supports OpenGL / DirectX Local Lighting with Infinite & Local Viewer. Up to 8 lights. Includes Range and Spot Attenuation, Includes DX7 color-per-vertex support.
- Supports Vertex Reuse capability for performance optimization of triangle lists
- Supports Back-Face Culling for performance optimization
- Supports polygon-id based shadow processing.

- Supports DirectX dual cone spot lights for DirectX lighting model.
- Supports normal re-normalization and constant rescale for DirectX/OpenGL lighting model.
- Supports separate and combined accumulation of diffuse and specular colors for DirectX/OpenGL lighting models.
- Supports derivation of alpha through lighting model calculations or directly from input diffuse color.

1.3.4 Motion Video Acceleration Features

- Video scaling and fully programmable YCrCb to RGB color space conversion for full-screen / full-speed video playback and fully adjustable color controls.
- Front and back end scalers plus capture port scaler to support multi-stream video for video conferencing and other applications.
- Front end scaler support for 8, 15, 16, and 32 bpp color depths.
- Back end overlay/scaler supports up to 8x4 tap filtering, and always ensures at least 4x2 tap filtering even in extreme cases. 4x4 tap is typical. Back-end scaler also supports upscaling and downscaling, filtered scaling of all supported YUV formats, RGB32 and RGB15/16, and filtered display of images up to 1920 pixels wide.
- Expanded line buffer allowing vertical filtering of native standard definition images.
- Enhanced MPEG-2 hardware decode acceleration, including support for both motion compensation and IDCT, to provide dramatically reduced CPU utilization without incurring the cost of a full MPEG-2 decoder. Also supports all format DTV/HDTV decode and top quality DVD with lowest CPU usage. This is superior to competing motion compensation solutions, including those marketed as ‘9-bit’ motion compensation.
- Integrated high performance iDCT and motion compensation allows MPEG-2 decode of all 18 ATSC formats including 1280x720p and 1920x1080i on standard speed CPUs. It also allows "timeshifting" of standard definition television in standard systems by ensuring the CPU has enough remaining power to perform real-time MPEG-2 compression while the M6 handles most of the MPEG-2 decompression load.
- Hardware DVD subpicture decoder with interpolating scaler and alpha compositor to provide optimal DVD subpicture quality in all display bit depths.
- Adaptive de-interlacing filter eliminates video artifacts caused by displaying interlaced video on non-interlaced displays, by analyzing image and using optimal

de-interlacing function on a per-pixel basis. Also can be programmed to other methods such as bob, weave, and ATI enhanced weave.

- Bi-directional bus mastering engine with full YC_rC_b planar mode support for superior MPEG-2 decode and video conferencing.
- Enhanced support for range based graphics and video keying for effective overlay of video and graphics.
- Ability to genlock to any broadcast video signal, eliminating synchronization problems.
- YC_rC_b to RGB color space converter with support for both packed and planar YC_rC_b (YC_rC_b422, YC_rC_b410, YC_rC_b420). Increased user control over color characteristics, and improved precision and gamma correction for brighter, richer color.
- YC_rC_b422, YC_rC_b410, YC_rC_b420, RGB32, RGB16/15 in back end scaler/overlay.
- Ability to reconstruct frames of field-based content when software indicates that content was originally progressive and has been converted via 3:2 pull down, provided that the decoder gives appropriate cues.
- Hardware mirroring for flipping mirror images in video conferencing systems.

1.3.5 Zoom Video Port Features

- ZV port (PCMCIA compliant with CCIR601 timing).
- Allows transfer of the video data directly into the frame buffer without loading down the PCI bus
- Dedicated video port guarantees video frame rates (30 frames per second)
- Maximum 40MHz, 16bpp YUV422 (PCMCIA specs 16MHz maximum)

1.3.6 Dual Display Features

General

- Dual independent displays (LCD/LCD, LCD/CRT, LCD/TV, CRT/TV)
- Two triple 10-bit palette DACs with gamma correction for true WYSIWYG color. Pixel rates up to 300 MHz standard.
- Resolution, refresh rates and display data can be completely independent.
- Primary display path supports VGA and accelerated modes, video overlay, hardware cursor, hardware icon and palette gamma correction.

- Secondary display path supports accelerated modes, video overlay, hardware cursor, hardware icon and palette gamma correction. However, it does not support VGA.
- Video genlocking supported for both CRTCs.
- Single video overlay using back-end scaler is switchable between displays.
- Supports two new graphics formats: 16bpp aRGB 4444 and 16bpp alpha and index 88. Also supports 8/15/16/24/32 bpp graphics formats with gamma correction in all modes.
- Stereoscopic display capability.
- Support for auxilary window signal.
- Support for up to 4k x 4k resolution display.
- Support for DDC1 and DDC2B+ for plug and play monitors, and AppleSense monitor detection support.
- 8-bit alpha blending of graphics and video overlay.
- Hardware cursor up to 64x64 pixels in 2bpp, full color AND/XOR mix, and full color 8-bit alpha blend.
- Hardware icon up to 128x128 pixels in 2bpp.
- Virtual desktop support.
- Support for flat panel displays (see section on Fixed Resolution Display below for details).

TV Out

An integrated TV encoder with on-chip triple DAC allows simultaneous CRT/LCD/TV output with these outstanding TV-out characteristics:

- 10-bit DAC with 8-tap filter producing scaled, flicker removed, artifact suppressed display on a PAL or NTSC TV with Composite, S-Video, and RGB outputs.
- Support for Macrovision 7.02 copy protection standard (required by DVD players) - a fully programmable timing capability, it will accommodate potential changes in the Macrovision algorithm without any hardware changes.

- YUV Direct/Passthrough mode for video/MPEG playback and DVD provides the best quality movie playback, it also allows titles to be displayed on TV with their original high quality and without any artifact from the TV-out circuit.
- Secondary display support for the RGB mode.

- 1024x768 32bpp support - improved from ImpactTV2 to support up to 1024x768 mode. Modes supported include the 800x600 and 16:9 type display such as 848x480, with user flexibility for moving and sizing the screen.
- Line 21 Closed Caption and Extended Data Service support for encoding in Vertical Blanking Interval (VBI) of TV signal.
- CGMS-A DVD copy management support in VBI through Line-20 and/or Extended Data Service (Line-21 Field 2).
- UV filtering based on colour averaging results in a sharper picture as well as reduced flicker.
- ATI's exclusive "Composite Dot Crawl" freeze option for PAL and NTSC to improve picture quality.
- TV-out power management support.

Features for Fixed Resolution (e.g. Flat Panel or Digital CRT) Display via integrated TMDS transmitter

- Supports DVI, DFP and VESA P&D interfaces with integrated TMDS transmitter.
- TMDS transmitter operates to 165 MHz and fully supports reduced blanking.
- Support for fixed resolution displays (e.g. panels) from VGA (640x480) to wide UXGA (1600x1200) resolution with full ratiometric expansion ability for source modes up to 1280x1024. Higher resolution panels and digital CRTs possibly supported. Contact ATI for details.
- Improved auto expansion.
- Optional auto-centering mode to display desktop at native size without ratiometric expansion.
- Support for VGA text modes in centering panel modes (up to approximately 165 MHz pixel frequency).
- Support for reduced blanking intervals, as defined by VESA.

1.3.7 Integrated LVDS

- Integrated dual 112MHz LVDS interface.
- Single/dual channel QXGA resolution TFT panels.
- 32bpp TFT (QXGA) using dual channel LVDS.
- 784 Mbps/channel with 112 MHz pixel clock rate.

- 3 pairs (+1 clock) and 4 pairs (+1 clock) modes for both single and dual channel LVDS.
- FPDI-2 compliant; compatible with receivers from National Semiconductor, Texas Instruments, and THine.
- OpenLDI compliant excluding DC balancing.
- LVDS eye pattern to improve testability of LVDS module.

1.3.8 Bus Support Features

- Comprehensive AGP support:
  - 2X and 4X mode operation.
  - Sideband Addressing.
  - AGP Texturing (Execute mode).
  - Both AGP reads and writes (without support for the ‘fast write’ capability defined in revision 2.0 of the AGP specification.
  - AGP 1X mode operation.
- PCI version 2.2 with full bus mastering and scatter / gather support.
- 3.3 V and 5 V PCI interfaces. 5 V PCI only compatible with systems that ensure bus signals do not rise above 3.3 V typical. This works with all current standard system chipsets from Intel and other major suppliers.
- Support for AGP Power Management via AGP Busy protocol (1.61 as well as Solano2-M 0.1).

1.3.9 Memory Support Features

- Supports a variety of memory configurations for bandwidths of up to 3.2 GB/s:
  - SDRAM or SGRAM may be used for all memory configurations (32 or 64-bit).
  - Single Data Rate (SDR), up to 200 MHz (1.6 GB/s at 64-bits).
  - Double Data Rate (DDR), up to 200 MHz (3.2 GB/s at 64-bits).
- Flexible graphics memory configurations: 8MB up to 128MB SDR/DDR SGRAM or SDR SDRAM.
- Memory upgrade via industry standard SO-DIMM, for reduced board area and higher memory speeds.

- Support for LVTTL and SSTL-2 memory interfaces.
- Does not support SGRAM "block write" feature.
- Does not support memory interfaces **less than** 8MB memory configurations.

1.3.10 Power Management Features

- Support for version 1.0 of the ACPI Specification and version 1.1 of the PCI Bus Power Management Interface Specification (PCI PMI).
- The Chip Power Management Support logic supports four device power states - On, Standby, Suspend and Off - defined for the OnNow Architecture. Each power state can be achieved by software control bits.
- Clocks to every major functional block are controlled by a unique dynamic clock switching technique which is completely transparent to the software. By turning off the clock to the block that is idle or not used at that point, the power consumption is significantly reduced during normal operation.
- Self-refresh SDRAM/SGRAM in Suspend mode
- No support pin or timer mode

1.3.11 PC Design Guide Compliance

M6 complies with all relevant sections of the current PC design guide specifications from Intel/Microsoft. It is fully compliant with PC99 and PC99a. It is also compliant with the current PC2001 proposal (v0.5).

1.3.12 Test Capability Features

The M6 has a variety of test modes and capabilities that provide a very high fault coverage and low DPM (Defect Per Million) ratio:

- Full scan implementation on the digital core logic which provides about 99% fault coverage through ATPG (Automatic Test Pattern Generation Vectors).
- Dedicated test logic for the on-chip custom memory macros to provide complete coverage on these modules.
- A JTAG test mode (which is not entirely compliant to the IEEE 1149.1 standard) in order to allow board level testing of neighboring devices.

- An EXORTREE test mode on all the digital I/O's to allow for proper soldering verification at the board level.
- An EXTEST test mode in order to allow board level testing by sampling the inputs and controlling the outputs of M6.
- Improved access to the analog modules and PLLs in the M6 in order to allow full evaluation and characterization of these modules.
- Improved IDDQ mode support to allow chip evaluation through current leakage measurements.

These test modes can be accessed through the settings on the instruction register of JTAG circuitry.

1.4 Display Modes

The modes below are based on the 300MHz DAC. Some modes may not be supported in all production driver releases.

1.4.1 2D Display Modes

Table 1-1 M6 2D Dispaly Modes

Display Screen Resolution	Refresh Rate (Hz)	Hor. Scan (KHz)	Pixel Clock (MHz)	Color Depth (bpp)		
				8	16	32
640x480	60	31.5	25.2	✓	✓	✓
	72	37.9	31.5	✓	✓	✓
	75	37.5	31.5	✓	✓	✓
	85	43.3	36.0	✓	✓	✓
	90	45.4	37.8	✓	✓	✓
	100	50.9	43.1	✓	✓	✓
	120	61.8	52.4	✓	✓	✓
	160	84.3	72.8	✓	✓	✓
	200	108.0	95.0	✓	✓	✓

Table 1-1 M6 2D Dispaly Modes (Continued)

Display Screen Resolution	Refresh Rate (Hz)	Hor. Scan (KHz)	Pixel Clock (MHz)	Color Depth (bpp)		
				8	16	32
800x600	60	37.9	39.9	✓	✓	✓
	70	43.7	45.5	✓	✓	✓
	72	48.1	50.0	✓	✓	✓
	75	46.9	49.5	✓	✓	✓
	85	53.7	56.3	✓	✓	✓
	90	56.8	60.0	✓	✓	✓
	100	63.6	68.1	✓	✓	✓
	120	77.1	83.9	✓	✓	✓
	160	105.4	116.4	✓	✓	✓
	200	135.0	149.0	✓	✓	✓
1024x768	60	48.4	65.0	✓	✓	✓
	70	56.5	75.0	✓	✓	✓
	72	57.6	78.4	✓	✓	✓
	75	60.0	78.8	✓	✓	✓
	85	68.7	94.5	✓	✓	✓
	90	72.8	100.1	✓	✓	✓
	100	81.4	113.3	✓	✓	✓
	120	98.7	139.0	✓	✓	✓
	140	116.6	164.2	✓	✓	✓
	150	125.7	176.9	✓	✓	✓
	160	134.8	192.0	✓	✓	✓
	200	172.8	246.1	✓	✓	*

Table 1-1 M6 2D Dispaly Modes (Continued)

Display Screen Resolution	Refresh Rate (Hz)	Hor. Scan (KHz)	Pixel Clock (MHz)	Color Depth (bpp)		
				8	16	32
1152x864	43	38.0	56.0	✓	✓	✓
	47	41.7	62.1	✓	✓	✓
	60	53.7	81.6	✓	✓	✓
	70	63.0	96.7	✓	✓	✓
	75	67.5	108.0	✓	✓	✓
	80	72.4	112.3	✓	✓	✓
	85	77.0	119.6	✓	✓	✓
	100	91.5	143.4	✓	✓	✓
	120	111.1	176.0	✓	✓	✓
	150	141.4	226.3	✓	✓	*
	160	151.6	242.6	✓	✓	*
1280x1024	60	64.0	108.0	✓	✓	✓
	70	74.6	128.9	✓	✓	✓
	74	79.0	138.5	✓	✓	✓
	75	80.0	135.0	✓	✓	✓
	85	91.1	157.5	✓	✓	✓
	90	97.0	169.2	✓	✓	✓
	100	108.5	190.9	✓	✓	✓
	120	131.6	233.7	✓	✓	*
1600x1200	52	64.2	137.7	✓	✓	✓
	58	71.9	155.4	✓	✓	✓
	60	75.0	162.0	✓	✓	✓
	66	82.2	178.9	✓	✓	✓
	75	93.8	202.5	✓	✓	✓
	76	95.2	208.7	✓	✓	✓
	85	106.3	229.5	✓	✓	*
	92	116.4	257.0	✓	✓	*
	100	127.1	280.6	✓	✓	*
1792x1344	60	83.5	203.0	✓	✓	✓
	75	105.2	259.3	✓	✓	✓
	85	119.9	295.5	✓	✓	*

Table 1-1 M6 2D Dispaly Modes (Continued)

Display Screen Resolution	Refresh Rate (Hz)	Hor. Scan (KHz)	Pixel Clock (MHz)	Color Depth (bpp)		
				8	16	32
1800x1440	60	89.4	219.5	✓	✓	✓
	70	104.9	249.9	✓	✓	*
1856x1392	60	86.5	218.6	✓	✓	✓
	75	109.0	277.2	✓	✓	*
1920x1080	60	67.0	172.7	✓	✓	✓
	70	78.6	205.1	✓	✓	✓
	75	84.6	220.6	✓	✓	✓
	80	90.4	237.4	✓	✓	✓
1920x1200	60	74.5	193.1	✓	✓	✓
	72	90.0	222.2	✓	✓	✓
	75	93.9	231.4	✓	✓	*
	76	95.2	245.0	✓	✓	*
	80	100.5	263.7	✓	✓	*
	85	107.1	282.7	✓	✓	*
1920x1440	60	89.4	234.5	✓	✓	*
	75	112.7	297.6	✓	✓	*
2048x1536	60	95.3	267.0	✓	✓	*
	70	111.9	315.2	✓	✓	*

* = Supported for all but 64 bit SDR memory as shown below

64-bit SDR Memory Speed	32bpp 2D Display Support
143 MHz	Up to 225 MHz pixel frequency
167 MHz	Up to 265 MHz pixel frequency
182 MHz	Up to 290 MHz pixel frequency
200 MHz	Up to 300 MHz pixel frequency

For 64-bit SDR memory, all display modes up to 300 MHz pixel frequency for 16bpp and 8bpp graphics are supported.

For 64-bit DDR memory, all graphics bit depths are supported for pixel frequencies up to 300 MHz. This holds for all memory speeds down to 110 MHz.

1.4.2 3D Modes

Table 1-2 3D Modes

Frame Buffer MB	Screen Resolution	Color depth Bit/Pixel	Front Buffer MB	Back Buffer MB	Z Buffer Depth[1]	Z buffer MB	Local Texture Memory[2] WZ MB	Local Texture Memory[2] W/O Z MB	Primary use of Configuration
8	640x480	16	0.59	0.59	16	0.59	6.24	6.83	
8	640x480	32	1.17	1.17	16	0.59	5.07	5.66	
8	800x600	16	0.92	0.92	16	0.92	5.25	6.17	
8	800x600	32	1.83	1.83	32	1.83	2.51	4.34	Value systems
8	1024x768	16	1.50	1.50	32	3.00	2.00	5.00	
8	1024x768	32	3.00	3.00	16	1.50	0.50	2.00	
8	1280x1024	16	2.50	2.50	16	2.50	0.50	3.00	
16	1280x1024	32	5.00	5.00	32	5.00	1.00	6.00	
16	1600x1200	16	3.66	3.66	32	7.32	1.35	8.68	Mainstream systems
32	1600x1200	32	7.32	7.32	32	7.32	10.0	17.35	
32	1920x1200	32	8.79	8.79	32	8.79	5.63	14.42	
64	2048x1536	32	12.0	12.0	32	12.0	28.0	40.0	PC Workstations

[1] 32 bit Z-buffer can optionally be configured as 24 bit Z-Buffer plus 8 bit Stencil Buffer.
[2] AGP configurations can use system memory for additional textures.

1.5 Software Features

- Dual processor support under OpenGL driver.
- BIOS ability to read EDID 1.1, 1.2, and 2.0.
- Ability to selectively enable and disable the panel monitor and analog monitor.
- Register-compatible with VGA standards, BIOS-compatible with VESA Super VGA.
- Full Open Firmware (IEEE 1275) support.
- Supports corporate manageability requirements such as DMI.
- 'Instantly Available' support.
- Full Write Combining support for maximum performance on advanced processors such as Pentium III and Athlon.
- Full-featured, yet simple Windows utilities:
  - Calibration utility for WYSIWYG color
  - Independent brightness control of desktop and overlay

- End user diagnostics

- SGI level III OpenGL licensee.
- Drivers meet Microsoft's rigorous WHQL criteria and are suitable for systems with the "Designed for Windows NT and Windows 98" and "Designed for Windows 2000" logos.
- Comprehensive OS and API support (see table below).
- Hot-key support - Mobile only.
- Extensive Power Management support.

Table 1-3 OS and API Support

Software Support	DOS	Win 3.x	Win 95	Win 98	NT 3.51	NT 4.0	Windows 2000	Mac OS	OS/2
2D Software Support [1]									
Accelerated Driver	VESA[2]	footnote 3	✓	✓	✓	✓	✓	✓	footnote 3
Video Software Support									
MS DirectDraw			✓	✓		✓	✓		
MS ActiveMovie/ Direct Show			✓	✓			✓		
MPEG-1 software playback			✓	✓		✓	✓	✓	
MPEG-2 software playback			✓	✓			✓	✓	
QuickTime acceleration								✓	
3D Software Support									
MS Direct3D			✓	✓			✓		
QuickDraw 3D RAVE								✓	
OpenGL			✓	✓		✓	✓		
AGP			✓	✓		footnote 4	✓		

1 - Additional third parties (including SCO Unix and UNIXWARE)
2 - Direct BIOS support
3 - Hardware cursor only
4 - NT 4.0 Service pack 3 supports AGP devices, but does not provide support for AGP texturing

This page intentionally left blank.

Chapter 2
Pin and Strap Descriptions

This chapter describes the signal distribution for the M6. All active low signals are shown with the suffix "#" or "*b*"(e.g., STOP#).

To link to a topic of interest, use the following list of hypertext linked cross references:

2.1 Pin Count by Functional Group

The following table shows the M6 pin count listed by functional grouping.

Table 2-1 Pin Count

Pin Group	Pin Count
Host Bus	71
Memory	107+4
Zoom Video / External TMDS	28
GPIO	14
LCD GPIO	3
LVDS	28
External SSC	2
Panel Control	2
TMDS / Flat Panel	18
CRT	14
TV Out	12
Test	1
ROM	1
PLLs & XTAL	6
Host Power	19
Memory I/O Power	19+1+10
Integrated memory Power	8
GP I/O Power	19
Core Power	24
Ground	74
TOTAL	**484**

2.2 Pin Assignment

2.2.1 M6 Pin Assignment Top View (Left Half)

	1	2	3	4	5	6	7	8	9	10	11	12	13
A	VSS	MPVDD	MPVSS	CLK1	CLK1_IN	CLK0	CLK0_IN	CKE	RASb	A(11)	A(8)	A(4)	A(1)
B	DQ(32)	VSS	CLKFB	CLK1b	CLK1b_IN	CLK0b	CLK0b_IN	CSb(1)	CSb(0)	A(10)	A(7)	A(3)	A(0)
C	DQ(33)	DQ(34)	VSS	VSS	VDDQM	VDDQM	VDDM	CASb	A(13)	A(9)	A(6)	A(2)	DQ(31)
D	DQ(35)	DQ(36)	VSS	VSS	VSS	VDDQM	VDDRH	Web	A(12)	VDDM	A(5)	VDDM	DQ(30)
E	DQ(37)	DQ(38)	VDDM	VSS	VSS	VDDR1	VDDR1	VDDC	VDDR1	VDDC	VDDR1	VDDC	VDDR1
F	DQ(39)	DQMb(4)	VDDQM	VDDM	VSS								
G	DQMb(5)	DQ(40)	DQ(41)	VDDQM	VDDR1								
H	DQ(42)	DQ(43)	DQ(44)	VDDR1	VDDC								
J	DQ(45)	DQ(46)	DQ(47)	QS(4)	VDDR1								
K	QS(5)	QS(6)	QS(7)	VDDR1	VDDC					VSS	VSS	VSS	VSS
L	DQ(48)	DQ(49)	DQ(50)	DQ(51)	VDDR1					VSS	VSS	VSS	VSS
M	DQ(52)	DQ(53)	DQ(54)	VDDR1	VDDC					VSS	VSS	VSS	VSS
N	DQ(55)	DQMb(6)	DQMb(7)	DQ(56)	VDDR1					VSS	VSS	VSS	VSS
P	DQ(57)	DQ(58)	DQ(59)	DQ(60)	VDDR1					VSS	VSS	VSS	VSS
R	DQ(61)	DQ(62)	DQ(63)	VDDR1	VDDC					VSS	VSS	VSS	VSS
T	MEMVMODE	VREF	GPIO(13)	GPIO(12)	VDDR3					VSS	VSS	VSS	VSS
U	GPIO(11)	GPIO(10)	GPIO(9)	VDDR3	VDDC					VSS	VSS	VSS	VSS
V	GPIO(8)	GPIO(7)	GPIO(6)	GPIO(5)	VDDR3								
W	GPIO(4)	GPIO(3)	GPIO(2)	VDDR3	VDDC								
Y	GPIO(1)	GPIO(0)	ROMCSb	ZV_LCDCNTL(0)	VDDR3								
AA	ZV_LCDCNTL(1)	ZV_LCDCNTL(2)	ZV_LCDCNTL(3)	ZV_LCDDATA(0)	VDDR3								
AB	ZV_LCDDATA(1)	ZV_LCDDATA(2)	ZV_LCDDATA(3)	ZV_LCDDATA(4)	VDDR3	VDDR3	VDDC	VDDC	BLONb	VDDR3	DIGON	VDDC	CRT2DDCCLK
AC	ZV_LCDDATA(5)	ZV_LCDDATA(6)	ZV_LCDDATA(7)	VDDR3	ZV_LCDDATA(23)	TESTEN	LTGIO(2)	TXOUT_L0N	TXOUT_L1N	TXOUT_L3N	TXOUT_U1N	TXCLK_UN	LVDDR
AD	ZV_LCDDATA(8)	ZV_LCDDATA(9)	ZV_LCDDATA(10)	ZV_LCDDATA(19)	ZV_LCDDATA(22)	LTGIO(1)	LTGIO(0)	TXOUT_L0P	TXOUT_L1P	TXOUT_L3P	TXOUT_U1P	TXCLK_UP	LVDDR
AE	ZV_LCDDATA(11)	ZV_LCDDATA(12)	ZV_LCDDATA(16)	ZV_LCDDATA(18)	ZV_LCDDATA(21)	SSIN	SSOUT	TXOUT_L2N	TXCLK_LN	TXOUT_U0P	TXOUT_U2P	TXOUT_U3N	V2SYNC
AF	ZV_LCDDATA(13)	ZV_LCDDATA(14)	ZV_LCDDATA(15)	ZV_LCDDATA(17)	ZV_LCDDATA(20)	LPVSS	LPVDD	TXOUT_L2P	TXCLK_LP	TXOUT_U0N	TXOUT_U2N	TXOUT_U3P	COMP_B
	1	2	3	4	5	6	7	8	9	10	11	12	13

Figure 2-1 M6 Top View (Left Half)

2.2.2 M6 Pin Assignment Top View (Right Half)

14	15	16	17	18	19	20	21	22	23	24	25	26	
DQ(29)	DQ(25)	DQMb(2)	DQ(20)	DQ(17)	QS(0)	DQ(14)	DQ(10)	DQMb(0)	DQ(5)	DQ(3)	DQ(2)	DQ(0)	A
DQ(28)	DQ(24)	DQ(23)	DQ(19)	DQ(16)	QS(1)	DQ(13)	DQ(9)	DQ(7)	DQ(4)	VDDQM	DQ(1)	AGPREF B66	B
DQ(27)	DQMb(3)	DQ(22)	DQ(18)	QS(3)	DQ(15)	DQ(12)	DQ(8)	DQ(6)	VDDM	VDDQM	AGPTEST	AD(1) B65	C
DQ(26)	VDDQM	DQ(21)	VDDM	QS(2)	VDDQM	DQ(11)	DQMb(1)	VDDQM	VDDM	AD(0) A65	AD(2) A63	AD(3) B63	D
VDDR1	VDDC	VDDR1	VDDC	VDDR1	VDDC	VDDR1	VDDR1	VDDP	AD(4) A62	AD(6) A60	AD(5) B62	AD(7) B60	E
								VDDP	CBEb(0)	AD_STBb(0)	AD_STB(0) B59	AD(8) B57	F
								VDDP	AD(9) A56	AD(11) A54	AD(10) B56	AD(12) B54	G
								VDDC	VDDP	AD(13) A53	AD(15) A51	AD(14) B53	H
								VDDP	PAR A50	STOPb A47	CBEb(1) B51	DEVSELb B46	J
VSS	VSS	VSS	VSS					VDDC	VDDP	TRDYb A46	FRAMEb A41	IRDYb B41	K
VSS	VSS	VSS	VSS					VDDP	AD(16) A39	AD(18) A38	CBEb(2) B39	AD(17) B38	L
VSS	VSS	VSS	VSS					VDDC	VDDP	AD(20) A36	AD(22) A35	AD(19) B36	M
VSS	VSS	VSS	VSS					VDDP	CBEb(3) A33	AD_STBb(1) A32	AD(21) B35	AD(23) B33	N
VSS	VSS	VSS	VSS					VDDP	AD(24) A30	AD(26) A29	AD_STB(1) B32	AD(25) B30	P
VSS	VSS	VSS	VSS					VDDC	VDDP	AD(28) A27	AD(27) B29	AD(29) B27	R
VSS	VSS	VSS	VSS					VDDP	AD(30) A26	SBA(7) A21	AD(31) B26	SBA(6) B21	T
VSS	VSS	VSS	VSS					VDDC	VDDP	SBA(5) A20	SB_STBb A18	SBA(4) B20	U
								VDDP	SBA(3) A17	SBA(1) A15	SB_STB B18	SBA(2) B17	V
								VDDC	VDDP	SERRb A14	SBA(0) B15	RBFb B12	W
								VDDP	ST(1) A10	GNTb A8	ST(2) B11	ST(0) B10	Y
								VDDP	RSTb A7	INTAb A6	REQb B8	PCICLK B7	AA
VDDC	VDDR3	VDDR3	VDDC	VDDR3	VDDC	VDDR3	VDDR3	VDDR3	VDDP	VDDP	STP_AGPb	AGP_BUSYb	AB
CRT2DDCDAT	A2VSSN	A2VSSN	VDDR3	TXVSSR	TXVDDR	DVIDDCDATA	AVSSQ	AUXWIN	VDDR3	VDDR3	VGADDCCLK	VGADDCDATA	AC
H2SYNC	A2VSSQ	A2VDDQ	A2VDD	TXVSSR	TXVDDR	DVIDDCCLK	HPD	AVSSN	AVDD	MONID(0)	MONID(1)	PVSS	AD
LVSSR	LVSSR	R2SET	TXVSSR	TXCM	TX0M	TX1M	TX2M	RSET	VSYNC	HSYNC	SUS_STATb	PVDD	AE
Y_G	C_R	TPVSS	TPVDD	TXCP	TX0P	TX1P	TX2P	B	G	R	XTALIN	XTALOUT	AF
14	15	16	17	18	19	20	21	22	23	24	25	26	

Figure 2-2 M6 Top View (Right Half)

2.3 AGP/PCI Host Bus Interface

Table 2-2 AGP/PCI Host Bus Interface

Pin Name	Type	Description
RSTb 1	I	Active Low PCI Reset, All PCI signals on the M6 will be tri-stated during its assertion This signal may be asserted or de-asserted asynchronously to the PCICLK, but it must be guaranteed to be clean and have bounce-free edges.
PCICLK	I	Bus Clock, this signal is used as a reference for all transactions on the PCI bus. Except for RSTb and INTAb, all PCI signals are sampled on the rising edge of this clock signal and all timing parameters are defined with respect to this rising edge. Itís frequency can be 33 - 66 Mhz depending on the system bus type (PCI 33 - PCI 66 - AGP)
AD(31:0)	I/O	Address/Data (31:0) A bus cycle consists of an address phase followed by one or more data phases. **PCI :** when the M6 is a target on the PCI bus, these signals are inputs for address read/writes and write data, and outputs for read data. This bus contains the address during the clock cycle in which FRAMEb is asserted (address phase), and it contains the data in the subsequent clock cycles. **AGP :** the M6 acts as an AGP master. Data is driven or received through the AD lines by the M6 after appropriate commands are sent to the host-to-PCI bridge via the side band address bus (SBA(7:0)) Note: in AGP mode, AD16 or AD17 (depending on the IDSELb strap setting) are also used for the IDSEL function.
C/BEb(3:0)	I/O	Bus Command/ Byte Enable(3:0) **PCI :** during the address phase of a transaction, these signals define the bus command (Int ack., spec. cycle, IO R/W, Mem R/W, Config R/W, etc.). During the data phase, they are used as Byte Enables (determine which byte on the AD line carries meaningful data) **AGP :** provide valid byte information during AGP write transactions and are driven by the master. They are driven to ë0000í by the target and ignored by the master (M6) during the return of AGP read data.
FRAMEb	I/O	Cycle Frame **PCI :** this signal is driven by the current master to indicate the beginning and duration of an access. It is asserted to indicate the beginning of a bus transaction. Data transfer will continue while this signal is asserted. When FRAMEb is deasserted, the transaction is in its final data phase. **AGP :** not used in AGP and kept in its deasserted state

Table 2-2 AGP/PCI Host Bus Interface (Continued)

Pin Name	Type	Description
IRDYb	I/O	Initiator (bus master) ready **PCI :** it indicates the ability of the current initiator (current bus master) to complete the current data phase of the transaction. During a write cycle, IRDYb indicates that valid data is present on the AD line. During a read cycle, it indicates that the master is ready to accept data. IRDYb is used in conjunction with the TRDYb signal. Wait cycles are inserted until both IRDYb and TRDYb are asserted. A data phase is completed on any clock where both IRDYb and TRDYb are sampled as asserted. **AGP :** for AGP writes, it indicates that the master is ready to provide all write data for the current write transaction. Once this signal is asserted for a write operation, the master is not allowed to insert wait states. For AGP reads, the assertion of this signal indicates that the master is ready to accept a subsequent block (32 bytes) of read data. the master is never allowed to insert a wait state during the initial block of a read transaction, but it may do so after subsequent block transfers. (there is no FRAMEb -- IRDYb relationship for AGP transactions) The target is allowed to insert wait states on block boundaries but not on individual data phases (for both Read and Write operations)
TRDYb	I/O	Target device ready **PCI :** it indicates the ability of the target to complete the current data phase of the transaction During a read cycle, TRDYb indicate that valid data is present on the AD line. During a write cycle, it indicates that the target is ready to accept data. TRDYb is used in conjunction with IRDYb. Wait cycles are inserted until both IRDYb and TRDYb are asserted. A data phase is completed on any clock where both IRDYb and TRDYb are sampled as asserted. **AGP :** for AGP reads, it indicates that the target is ready to provide read data for the entire transaction (when transaction can complete within four clocks) or is ready to transfer a (initial or subsequent) block of data when the transfer requires more than four clocks to complete. The target is allowed to insert wait states after each block transfers on both read and write transaction
DEVSELb	I/O	Device select **PCI :** when actively driven, it indicates that the driving device (target) has decoded its address as the target of the current access. As an input to other devices and the current master, it indicates whether any device on the bus has been selected. **AGP :** not used in AGP and kept in its deasserted state

Table 2-2 AGP/PCI Host Bus Interface (Continued)

Pin Name	Type	Description
STOPb	I/O	Target transaction termination request **PCI :** it indicates that the current target is requesting the master to stop the current transaction **AGP :** not used in AGP and kept in its deasserted state
PAR	O	Parity bit for AD(31:0) and C/BEb(3:0) **PCI :** parity is even across the AD and C/BEb lines. It means that PAR = 1 when the count of the number of ë1sí on the AD, C/BEb and PAR line is even. Parity generation is required by all PCI agents. PAR is stable and valid one clock after the address phase. For data phases, PAR is stable and valid one clock after either IRDYb is asserted on a write transaction or TRDYb is asserted on a read transaction. Once PAR is valid, it remains valid until one clock after the completion of the current data phase. PAR has the same timing as the AD line but delayed by one clock. The master drives PAR for address and write data phases and the target drives PAR for read data phases. **AGP :** not used in AGP but must be actively driven by the current owner of the AD bus
INTAb	O	Interrupt request line **PCI and AGP :** used to request an interrupt. Itís a shareable, level sensitive, active low signal. INTAb is for a single function device
REQb	I/O	PCI Bus Master Request signal to arbiter **PCI and AGP :** this signal indicates to the arbiter that this agent desires the use of the bus. This is a point to point signal (ie. each master has its own REQb line)
GNTb	I	PCI Bus Master Grant signal from arbiter **PCI :** this signal indicates to the agent that access to the bus has been granted by the arbiter. This is a point to point signal (ie. each master has its own REQb line) **AGP :** same as PCI but used in combination with the ST signals. the additional information provided by the ST lines indicates whether the master is the recipient of previously requested read data (high or low priority), or whether it is to provide write data (high or low priority) for a previously enqueued write command, or whether it has been given permission to start a bus transaction (AGP or PCI)

Table 2-2 AGP/PCI Host Bus Interface (Continued)

Pin Name	Type	Description
ST(2:0)	I	AGP Status bus **AGP :** these signals provide information from the arbiter to the master on what it may do. The ST lines have meaning to the master only when that masterís GNTb is asserted. When GNTb is not asserted, these signals have no meaning and must be ignored
SBA7/IDSEL	I/O	AGP Sideband Address port bit 7 **or** PCI Initialization device select (in PCI mode) **PCI :** it is used as a chip select during configuration read and write cycles **AGP :** AGP sideband address port bit 7
SBA(6:0)	O	Sideband Address port for AGP1X/2X support **AGP :** itís an additional bus used to pass requests (address and command) to the target from the master. Note : the M6 does not use the PIPEb mechanism to enqueue requests, it uses the SBA lines to enqueue requests to the arbiter.
RBFb	O	AGP Read buffer full **AGP :** this signal indicates whether the master is ready to accept previously requested low priority read data or not. When asserted, the arbiter is not allowed to initiate the return of low priority read data to the master.
AD_STB(1:0)	I/O	AGP-133 Address strobe **AGP :** AD_STB0 and AD_STB1 provide timing for AGP2x data transfer mode on respectively AD(15:0) and AD(31:16). The agent that is providing data drives this signal.
SB_STB	I/O	Sideband Strobe for AGP1X/2X support **AGP :** this signal provides timing for the SBA lines (when supported) and is always driven by the master. When the side band strobe has been idle, a sync. cycle need to be performed before a request can be enqueued.
AD_STBb(1:0)	I/O	AGP-133 Address strobe differential complement **AGP :** differential complement of AD_STB(1:0)
SB_STBb	I/O	Sideband Strobe differential complement **AGP :** differential complement of SB_STB

Table 2-2 AGP/PCI Host Bus Interface (Continued)

Pin Name	Type	Description
AGPTEST	I	External fixed reference **AGP4X/2X(1.5V)**: the compensator requires an external fixed reference to compare the strength of the chip against. This fixed reference is a resistor to ground, connected to AGPTEST. The compensator will drive the resistor with an output buffer in the AGPTEST pad, and measure the voltage. This voltage is an indication of the strength of the output driver. The compensator will adjust it accordingly. Resistor value should be 45 ohm +/-1% **PCI/AGP2X(3.3V)**: Unused. Leave this pin unconnected
AGPREF	I	Reference Voltage for differential receivers **AGP4X/2X(1.5V):** this voltage is set to VDDQ/2. All the differential receivers have an internal VREF available. The use of internal or external VREF is determined by whether VDDQ=3.3V or VDDQ=1.5V, respectively. **PCI/AGP2X(3.3V)**: Unused. Should be tied low
SERRb	O	**PCI :** System error signal to the PCI Bus, this is intended to be used for debug only. Full SERR support such as register support in configuration space, and reception of external SERR conditions is not intended. **Do not connect this signal on production boards.** This pin is also reserved for WBFb if it is ever required by future desgins.

2.4 Bus Power Management Interface

Table 2-3 Bus Power Management

Pin Name	Type	Description
STP_AGPb	I	Power management signal for AGP bus. **AGP :** graphics controller monitors this signal to find out when the CPU is about to enter S0/C3, S1, S2, S3 states. The southbridge generates this signal.
AGP_BUSYb	O	Power management signal for AGP bus. **AGP :** When asserted (active low), it indicates that the AGP device is currently busy and the AGP clock should not be stopped (meaning that the Host clock cant be stopped). The operating system should then transition into the C2 state instead of the C3 state. When de-asserted (active high), it indicates that the AGP device is not running any cycles and the AGP clock could be stopped.
SUS_STATb	I	Provides indication when AGP clock is about to stop. Should be connected to ***SUS_STAT#*** signal from the chipset.

Table 2-4 Signals Used by Various Host Buses

Signal Name	PCI	AGP 1X or 2X	AGP 4X
AD(31:0)	AD(31:0)	AD(31:0)	AD(31:0)
PCICLK	CLK	CLK	CLK
RST#	RST#	RST#	RST#
IRDY#	IRDY#	IRDY#	IRDY#
FRAME#	FRAME#	FRAME#	FRAME#
TRDY#	TRDY#	TRDY#	TRDY#
DEVSEL#	DEVSEL#	DEVSEL#	DEVSEL#
STOP#	STOP#	STOP#	STOP#
PAR	PAR	PAR	PAR
C/BE#(3:0)	C/BE#(3:0)	C/BE#(3:0)	C/BE#(3:0)
INTA#	INTA#	INTA#	INTA#
REQ#	REQ#	REQ#	REQ#
GNT#	GNT#	GNT#	GNT#
SB_STB		SB_STB	SB_STB
ST(2:0)		ST(2:0)	ST(2:0)
SBA7	IDSEL	SBA(7)	SBA(7)
SBA(6:0)		SBA(6:0)	SBA(6:0)
RBF#		RBF#	RBF#
AD_STB(1:0)		AD_STB(1:0)	AD_STB(1:0)
SB_STB#			SB_STB#
AD_STB#(1:0)			AD_STB#(1:0)
AGPREF		AGPREF	AGPREF
AGPTEST		AGPTEST	AGPTEST
SERR#	SERR#	SERR#	SERR#
AGP_BUSY#		AGP_BUSY#	AGP_BUSY#
STP_AGP#		STP_AGP#	STP_AGP#
SUS_STAT#		SUS_STAT#	SUS_STAT#

Note:

- In PCI mode, IDSEL will be supported through the SBA7 pin. In AGP mode, IDSEL will be multiplexed through pin AD16 or AD17 depending on the setting of the 'idselb' strap (see *Section 2.2.2 on page 2-23*).
- For PCI implementations, leave all unused AGP only pins as no-connects (open). PCI interface is not 5V tolerant.

- SUS_STAT# pin is used in addition to the STP_AGP# and AGP_BUSY# to inform ASIC when AGP clock is about to stop. It should be connected to SUS_STAT# signal (active low) from the chipset. All three Power Management signals are 3.3V signals regardless of the bus voltage.

2.5 Memory Interface (SGRAM, SDRAM)

Table 2-5 Memory Interface

Pin Name	Type	Description
DQ(63:0)	I/O	Memory Data Bus Supports SSTL2 and SSTL3 (DDR), and LVTTL (SDR)
DQMb(7:0)	O	Byte enables Memory data byte enables for write cycles
ADDR(13:0)	O	Memory Address Bus Provide multiplexed row and column addresses to the S(D/G)RAMs A(13) is always BA(0). A(12) is BA(1) for 4 bank S(D/G)RAMs and A(12) for 2 bank S(D/G)RAMs.
CSb(1:0)	O	Chip selects and upper row addresses to the S(D/G)RAMs
QS(7:0)	I/O	DDR data strobes Channel A, these strobes are used to latch data into the chip and the DDR S(D/G)RAMs.
RASb	O	Row Address Strobe
CASb	O	Column Address Strobe
WEb	O	Write enable
CKE	O	Clock enable control
CLK0	I/O	Memory clock 0
CLK0b	I/O	Memory clock 0 bar, required for external feedback for DLLs
CLK1	I/O	Memory clock 1
CLK1b	I/O	Memory clock 1 bar, required for external feedback for DLLs
CLKFB	O	Feedback clock
CLK0_IN	I	Internal SDRAM memory clock 0 (lower 32-bits)
CLK0b_IN	I	Internal SDRAM memory clock 0 bar (lower 32-bits)
CLK1_IN	I	Internal SDRAM memory clock 1 (upper 32-bits)
CLK1b_IN	I	Internal SDRAM memory clock 1 bar (upper 32-bits)
VREF	I	Reference voltage (1.25V Typ. for SSTL-2 / 0.5 * VDD) (1.5V Typ. for SSTL-3 / 0.45 * VDD) Note: if the differential signaling intf. is not used, this pin must be connected to the memory IOís VDDR (3.3V or 2.5V)

Table 2-5 Memory Interface (Continued)

Pin Name	Type	Description
MEMVMODE	I	Voltage value for S(D/G)RAM chips: 0 or 0V for VDDR 3.3V 1 or VDDR for VDDR 2.5V Pin has internal pulldown for default of VDDR 3.3V

2.6 Zoom Video Port / External TMDS Interface

Table 2-6 Zoom Video Port / External TMDS Interface

Pin Name	Type	Description
ZV_LCDCNTL (3:0) ZV_LCDDATA(23:0)	I/O	Zoom Video Port , **Or** External TMDS , **Or** TestBus output, **Or** JTAG control Refer to Chapter 4 for pin name and signal name mappings

2.7 General Purpose I/O Interface

Table 2-7 General Purpose I/O Interface

Pin Name	Type	Description
GPIO(13:0)	I/O	External TMDS, **Or** Serial ROM, **Or** Parallel ROM, **Or** Input TestBus, **And** straps Refer to Chapter 4 for GPIO multiplexing and straps

2.8 LCD General Purpose I/O Interface

Table 2-8 LCD General Purpose I/O Interface

Pin Name	Type	Description
LTGIO(2:0)	I/O	Panel ID detection (could be used for internal panel DDC detection)

2.9 LVDS Interface

Table 2-9 LVDS Interface

Pin Name	Type	Description
TXOUT_U0N	O	LVDS upper data channel 0 (-) Transmitting at a bit rate of 7x pixel clock, up to 85MHz pixel clock. Only used in dual-channel LVDS mode.
TXOUT_U0P	O	LVDS upper data channel 0 (+) Transmitting at a bit rate of 7x pixel clock, up to 85MHz pixel clock. Only used in dual-channel LVDS mode.
TXOUT_U1N	O	LVDS upper data channel 1 (-) Transmitting at a bit rate of 7x pixel clock, up to 85MHz pixel clock. Only used in dual-channel LVDS mode.
TXOUT_U1P	O	LVDS upper data channel 1 (+) Transmitting at a bit rate of 7x pixel clock, up to 85MHz pixel clock. Only used in dual-channel LVDS mode.
TXOUT_U2N	O	LVDS upper data channel 2 (-) Transmitting at a bit rate of 7x pixel clock, up to 85MHz pixel clock. Only used in dual-channel LVDS mode.
TXOUT_U2P	O	LVDS upper data channel 2 (+) Transmitting at a bit rate of 7x pixel clock, up to 85MHz pixel clock. Only used in dual-channel LVDS mode.
TXOUT_U3N	O	LVDS upper data channel 3 (-) Transmitting at a bit rate of 7x pixel clock, up to 85MHz pixel clock. Only used in dual-channel LVDS mode.
TXOUT_U3P	O	LVDS upper data channel 3 (+) Transmitting at a bit rate of 7x pixel clock, up to 85MHz pixel clock. Only used in dual-channel LVDS mode.
TXCLK_UN	O	LVDS upper clock channel (-) Transmitting at pixel clock rate, up to 85MHz pixel clock. Only used in dual-channel LVDS mode.
TXCLK_UP	O	LVDS upper clock channel (+) Transmitting at pixel clock rate, up to 85MHz pixel clock. Only used in dual-channel LVDS mode.

Table 2-9 LVDS Interface (Continued)

Pin Name	Type	Description
TXOUT_L0N	O	LVDS lower data channel 0 (-) Transmitting at a bit rate of 7x pixel clock, up to 85MHz pixel clock. This channel is used as the transmitting channel in single channel LVDS mode.
TXOUT_L0P	O	LVDS lower data channel 0 (+) Transmitting at a bit rate of 7x pixel clock, up to 85MHz pixel clock. This channel is used as the transmitting channel in single channel LVDS mode.
TXOUT_L1N	O	LVDS lower data channel 1 (-) Transmitting at a bit rate of 7x pixel clock, up to 85MHz pixel clock. This channel is used as the transmitting channel in single channel LVDS mode.
TXOUT_L1P	O	LVDS lower data channel 1 (+) Transmitting at a bit rate of 7x pixel clock, up to 85MHz pixel clock. This channel is used as the transmitting channel in single channel LVDS mode.
TXOUT_L2N	O	LVDS lower data channel 2 (-) Transmitting at a bit rate of 7x pixel clock, up to 85MHz pixel clock. This channel is used as the transmitting channel in single channel LVDS mode.
TXOUT_L2P	O	LVDS lower data channel 2 (+) Transmitting at a bit rate of 7x pixel clock, up to 85MHz pixel clock. This channel is used as the transmitting channel in single channel LVDS mode.
TXOUT_L3N	O	LVDS lower data channel 3 (-) Transmitting at a bit rate of 7x pixel clock, up to 85MHz pixel clock. This channel is used as the transmitting channel in single channel LVDS mode.
TXOUT_L3P	O	LVDS lower data channel 3 (+) Transmitting at a bit rate of 7x pixel clock, up to 85MHz pixel clock. This channel is used as the transmitting channel in single channel LVDS mode.

Table 2-9 LVDS Interface (Continued)

Pin Name	Type	Description
TXCLK_LN	O	LVDS lower clock channel (-) Transmitting at pixel clock rate, up to 85MHz pixel clock. This channel is used as the transmitting channel in single channel LVDS mode.
TXCLK_LP	O	LVDS lower clock channel (+) Transmitting at pixel clock rate, up to 85MHz pixel clock. This channel is used as the transmitting channel in single channel LVDS mode.

2.10 LVDS Power and Ground Interface

Table 2-10 Video Capture Interface

Pin Name	Type	Description
LPVDD	I	Powering LVDS PLL macro **(1.8V)**
LPVSS	O	LVDS PLL macro ground pin
LVDDR (x2)	I	Powering LVDS IOs. **(1.8V)**
LVSSR (x2)	O	LVDS IO ground pin

2.11 External SSC

Table 2-11 External SSC Interface

Pin Name	Type	Description
SSIN	I	External SSC Clock In (output from SSC)
SSOUT	O	External SSC Clock Out (input to SSC)

2.12 Panel Control

Table 2-12 Panel Control Interface

Pin Name	Type	Description
DIGON	O	Controls Panel Digital Power On/Off
BLONb	O	Control Backlight On/Off

2.13 TMDS Interface

Table 2-13 TMDS Interface

Pin Name	Type	Description
TX0P	A-I/O	TMDS data channel 0 (+) Transmitting at a bit rate of 10x pixel clock, up to 165Mhz pixel clock.
TX0M	A-I/O	TMDS data channel 0 (-) Transmitting at a bit rate of 10x pixel clock, up to 165Mhz pixel clock.
TX1P	A-I/O	TMDS data channel 1 (+) Transmitting at a bit rate of 10x pixel clock, up to 165Mhz pixel clock.
TX1M	A-I/O	TMDS data channel 1 (-) Transmitting at a bit rate of 10x pixel clock, up to 165Mhz pixel clock.
TX2P	A-I/O	TMDS data channel 2 (+) Transmitting at a bit rate of 10x pixel clock, up to 165Mhz pixel clock.
TX2M	A-I/O	TMDS data channel 2 (-) Transmitting at a bit rate of 10x pixel clock, up to 165Mhz pixel clock.
TXCP	A-I/O	TMDS clock channel (+) Transmitting at pixel clock rate, up to 165Mhz pixel clock
TXCM	A-I/O	TMDS clock channel (-) Transmitting at pixel clock rate, up to 165Mhz pixel clock
TPVDD	I	Powering TMDS PLL macro **(1.8V)**
TPVSS	A-Gnd	TMDS PLL macro ground pin
TXVDDR(x2)	I	Power TMDS IOs. **(1.8V)**
TXVSSR(x3)	O	TMDS IO ground pins
DVIDDCDATA	I/O	DDC pin used for Panel ID; SDA functionality for TMDS
DVIDDCCLK	I/O	DDC pin used for Panel ID; SCL functionality for TMDS
HPD	I	Panel detection; Input pin that monitors if the voltage is bigger than 2.0V on the hot-plugging line.

2.14 DAC (CRT) Interface

Table 2-14 DAC (CRT) Interface

Pin Name	Type	Description
R	A-O	Red for monitor Analog DAC output, designed to drive a 37.5 Ohm equivalent load, driving the Red pin of the monitor (37.5 Ohm = 75 Ohm pull-down resistor on board in parallel with the 75 Ohm CRT load/Impedance).
G	A-O	Green for monitor Analog DAC output, designed to drive a 37.5 Ohm equivalent load, driving the Green pin of the monitor (37.5 Ohm = 75 Ohm pull-down resistor on board in parallel with the 75 Ohm CRT load/Impedance).
B	A-O	Blue for monitor Analog DAC output, designed to drive a 37.5 Ohm equivalent load, driving the Blue pin of the monitor (37.5 Ohm = 75 Ohm pull-down resistor on board in parallel with the 75 Ohm CRT load/Impedance).
HSYNC	I/O	Horizontal sync for Monitor This signal requires an on board TTL buffer (eg. LS125)
VSYNC	I/O	Vertical sync for Monitor This signal requires an on board TTL buffer (eg. LS125)
MONID(1:0)	I/O	MONID pins
VGADDCDATA	I/O	DDC data pin for CRT.
VGADDCCLK	I/O	DDC pin / SCL for CRT
AUXWIN	I/O	Dual functionality: Special output pin for Apple or Geyserville interrupt pin for Wintel platforms.
AVDD	A-Pwr	DAC VDD (1.8V) Dedicated power for CRT DAC. Effort should be made at the board level to provide as clean a power as possible to this pin to avoid noise injection in the DAC which in term can affect the display quality. Adequate decoupling should be provided between this pin and AVSS.

Table 2-14 DAC (CRT) Interface (Continued)

Pin Name	Type	Description
AVSSN	A-Gnd	DAC VSS Dedicated ground for CRT DAC. Effort should be made at the board level to provide as clean a ground as possible to this pin to avoid noise injection in the DAC which in term can affect the display quality. Adequate decoupling should be provided between this pin and AVDD.
AVSSQ	A-Gnd	Band Gap Ref. VSS Dedicated ground for the CRT Band Gap Reference (DAC). Effort should be made at the board level to provide as clean a ground as possible to this pin to avoid noise injection in the DAC which in term can affect the display quality. Adequate decoupling should be provided between this pin and AVDD.
RSET	A-O	Internal DAC reference Used to set the full scale DAC current through a high precision resistor (1%) of 422 Ohm (preliminary value) placed between this pin and AVSS.

2.15 DAC2 (TV/CRT2) Interface

Table 2-15 DAC2 (TV/CRT2) Interface

Pin Name	Type	Description
Y_G	A-O	SVID Y output for TV out, Or SCART Green output for TV out, Or Green for 2nd CRT Monitor
C_R	A-O	SVID C output for TV out, Or SCART Red output for TV out, Or Red for 2nd CRT Monitor
COMP_B	A-O	Composite Video for TV out, Or SCART Blue output for TV out, Or Blue for 2nd CRT Monitor
H2SYNC	I/O	Sync signal for TV SCART out, Or Horizontal Sync for 2nd CRT when TV out is not used.
V2SYNC	I/O	Vertical Sync for 2nd CRT when TV out is not used.
CRT2DDCCLK	I/O	DDC pin / SCL for second CRT or external TMDS Tx
CRT2DDCDAT	I/O	DDC pin / SDA for second CRT or external TMDS Tx

Table 2-15 DAC2 (TV/CRT2) Interface (Continued)

Pin Name	Type	Description
A2VDD	A-Pwr	DAC2 VDD (2.5V)
A2VDDQ	A-Pwr	DAC2 Band Gap Ref. Voltage (1.8V)
A2VSSQ	A-Gnd	DAC2 VSS (quiet ground; use for Band Gap)
A2VSSN	A-Gnd	DAC2 VSS (noisy ground; used as current dump)
R2SET	A-O	Internal Reference for second DAC

2.16 Test Interface

Table 2-16 Video Capture Interface

Pin Name	Type	Description
TESTEN	I	Test mode enable (Other 4 signals are muxed on ZV_LCDCNTL); must be connected to ground for normal operation. Used as TRSTb in JTAG interface.

2.17 ROM Interface

Table 2-17 ROM Interface

Pin Name	Type	Description
ROMCSb	O	BIOS ROM Chip Select Used to enable the Rom for Rom Read and Write (if flashrom) operations.

2.18 PLLs and Crystal Interface

Table 2-18 PLL and Crystal Interface

Pin Name	Type	Description
XTALIN	I	PLL Reference Clock or MXCLK source (14.318 - 29.4989 Mhz) (3.3V or 2.5V Input level)
XTALOUT	I/O	PLL Reference Clock (3.3V or 2.5V Input level) A series resonant crystal can be connected between these two pins to provide the reference clock for the internal PLLs of P6 / M6. An external LVTTL (3.3/2.5V) Oscillator can also be connected to XTALIN to provide the reference clock. In order to provide reliable functionality, proper video synchronization and high quality display, it is recommended that the crystal/oscillator should have as small an error (50 ppm) and jitter as possible, with a balanced duty cycle (55-45 worst case). Xtal characteristics (also valid for Oscillators): -Frequency : 14.31818 Mhz / 29.498928 Mhz (if with TVout) -Accuracy : 50 ppm -Duty cycle (worst case) : 45-55 (max) -Jitter : 500 ps (max) cycle to cycle -Voltage supply : 2.5V / 3.3V
PVDD	A-Pwr	Phase Lock Loop Power (1.8V) Dedicated power pin for M6 PLLs. Effort should be made at the board level to provide as clean a power as possible to this pin to avoid noise injection in the PLLs which in term can affect the display quality and functional reliability of the P6 / M6. Adequate decoupling should be provided between this pin and PVSS.
PVSS	A-Gnd	Phase Lock Loop Ground Dedicated ground for the M6 PLLs. Effort should be made at the board level to provide as clean a ground as possible to this pin to avoid noise injection in the PLLs which in term can affect the display quality and functional reliability of the Rage 5. adequate decoupling should be provided between this pin and PVDD.

Table 2-18 PLL and Crystal Interface (Continued)

Pin Name	Type	Description
MPVDD	A-Pwr	Memory Phase Lock Loop Power (1.8V) Dedicated power pin for the M6 memory PLL. Effort should be made at the board level to provide as clean a power as possible to this pin to avoid noise injection in the PLLs which in term can affect the display quality and functional reliability of the P6 / M6. adequate decoupling should be provided between this pin and PVSS.
MPVSS	A-Gnd	Memory Phase Lock Loop Ground Dedicated ground for the M6 Memory PLL. Effort should be made at the board level to provide as clean a ground as possible to this pin to avoid noise injection in the PLLs which in term can affect the display quality and functional reliability of the Rage 5. adequate decoupling should be provided between this pin and PVDD.

2.19 Host Power Interface

Table 2-19 Host Power Interface

Pin Name	Type	Description
VDDP	Pwr	1.5V/3.3V - PCI / AGP IO power for the AGP/PCI pins

2.20 Memory Power Interface

Table 2-20 Memory Power Interface

Pin Name	Type	Description
VDDR1 (memory)	Pwr	2.5V/3.3V (DDR/SDR) IO power for the memory bus. In case of M6, it should be 2.5V (same as VDDQM).
VDDM	Pwr	2.5V Core power for integrated memory.
VDDQM	Pwr	2.5V Memory die IO power.

Table 2-20 Memory Power Interface

Pin Name	Type	Description
VDDRH	Pwr	2.5V/3.3V (DDR/SDR) Dedicated power pin for memory clock pads. It should have the same voltage level as VDDR1

2.21 I/O Power Interface

Table 2-21 I/O Interface

Pin Name	Type	Description
VDDR3 (all other digital)	Pwr	3.3V IO power for other pins

2.22 Core Power Interface

Table 2-22 Core Power Interface

Pin Name	Type	Description
VDDC	Pwr	1.8V dedicated core power, provides power to the M6 internal logic

2.23 Ground Interface

Table 2-23 Ground Interface

Pin Name	Type	Description
VSS	Gnd	Ground

2.24 M6 Straps

2.24.1 Pin Based Straps

Table 2-24 Pin Based Straps

Strap	Pin	Description	Default
ID_DISABLE	GPIO(8)	0- Normal operation 1- Shuts the chip down by not responding to any config cycles. In a system with two graphics chips, one on the motherboard, the other on add-in card, this strap can be used to disable one of the two through a jumper.	0 (the chip will respond) (**internal pull-down**)
VGA_DISABLE	GPIO(7)	0- VGA controller capability enabled. 1- The device will not be recognized as the systems VGA controller.	0 (enable) (**internal pull-down**)
BUSCFG(2:0)	GPIO(6:4)	Controls bus type, CLK PLL select, and IDSEL. 000 1.5V bus -> AGP 4x, PLL clk, IDSEL=AD16 000 3.3V bus -> AGP 1x/2x, PLL clk, IDSEL=AD16 001 1.5V bus -> AGP 4x, PLL clk, IDSEL=AD17 001 3.3V bus -> AGP 1x/2x, PLL clk, IDSEL=AD17 010 1.5V bus -> AGP 1x/2x, PLL clk, IDSEL=AD16 010 3.3V bus -> AGP 1x/2x, PLL clk, IDSEL=AD16 011 1.5V bus -> AGP 1x/2x, PLL clk, IDSEL=AD17 011 3.3V bus -> AGP 1x/2x, PLL clk, IDSEL=AD17 100 PCI 66 MHz, PLL clk 101 PCI 33 MHz, 3.3V, REF clk 110 1.5V bus -> AGP 1x, REF clk, IDSEL=AD16 110 3.3V bus -> AGP 1x, REF clk, IDSEL=AD16 111 1.5V bus -> AGP 1x, REF clk, IDSEL=AD17 111 3.3V bus -> AGP 1x, REF clk, IDSEL=AD17 Note that for AGP configurations GPIO(4) acts as the IDSEL strap. For PCI it acts as the PLL bypass (33 or 66 MHz) strap.	000 (AGP 4x) (**internal pull-down**)
AGPFBSKEW(1:0)	GPIO(1:0)	AGP 1x clock feedback phase adjustment wrt refclk (cpuclk) 00 refclk slightly earlier than feedback 01 refclk 1 tap earlier than feedback 10 refclk 1 tap later than feedback 11 refclk 2 taps earlier than feedback clock	00 (**internal pull-down**)
X1CLK_SKEW(1:0)	GPIO(3:2)	Clock phase adjustment between x1clk and x2clk 00 - 0 tap delay 01 - 1 tap delay 10 - 2 taps delay 11 - 3 taps delay	00 (no skew) (**internal pull-down**)

Table 2-24 Pin Based Straps (Continued)

Strap	Pin	Description	Default
ROMIDCFG(2:0)	GPIO(13:11)	If no ROM attached, controls chip IDs. If ROM attached, identifies ROM type. *GPIO[13:11]* 000 No ROM, CHG_ID = 0 001 No ROM, CHG_ID = 1 010 reserved 011 reserved 100 Parallel ROM, chip IDs from ROM 101 Serial AT25F1024, chip IDs from ROM 110 Serial ST ROM, chip IDs from ROM 111 Serial ISSI ROM, chip IDs from ROM **Chip IDs**: Chip ID is based on CHG_ID strap: 0 No ROM, ID = **LY** or (0x4C59) 1 No ROM, ID = **LZ** or (0x4C5A)	000 (**internal pull-down)**

Notes on Pin Based Straps:

For straps which must be set on the board, the use of 4.7 kOhm (Min) to 10 kOhm (Max) resistors is recommended (for pull-ups to power (3.3V) or pull downs to ground). 4.7 kOhm provides more noise immunity whereas 10 kOhm will result in lower static power dissipation.

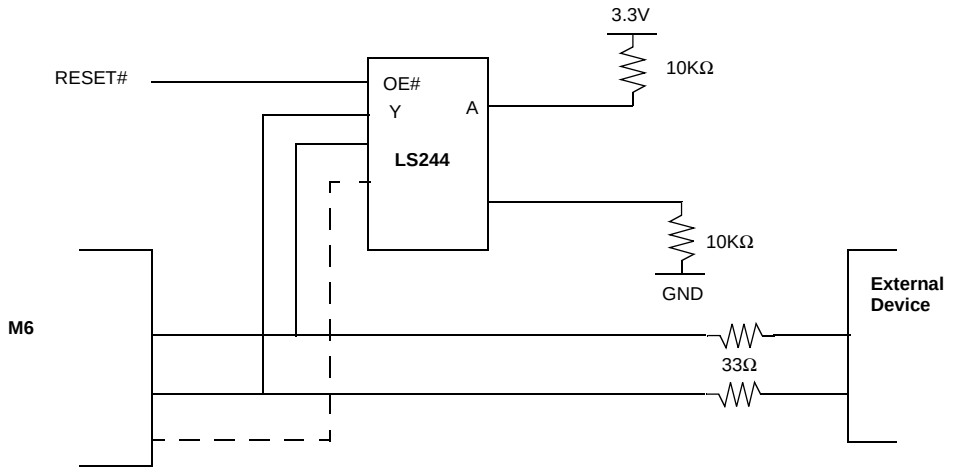

Figure 2-3 Implementation of Board Level Buffers

This circuit should not be needed if TVODATA and TVOCON connect only to ATI devices (i.e. RAGE THEATER), and not to any non-ATI devices and/or off board connectors or headers.

Most video encoders and external connectors/headers will only attach to TVODATA(9:2). This means one octal LS244 should be enough to force all 8 straps on these lines. TVOCON and TVODATA(1:0) are reserved for future versions of RAGE THEATER, and therefore should be left open except for the strap logic on most initial M6 circuit boards. In other words these three pins should not need this LS244 circuit.

If it is to be used off the circuit board, the STEREOSYNC pin should be buffered with an LS125 or equivalent. e.g. if the VESA Stereo display connector is populated. This will prevent external devices from interfering with the strap value floating according to the internal pull-down and potential external pull-up during reset. If STEROSYNC is not used in a given board design, the LS125 is not required.

For straps that must be set on the board, the use of 4.7 kΩ (min) to 10 kΩ (max) resistors is recommended (for pull-ups to power (3.3V) or pull downs to ground). 4.7 kΩ provides more noise immunity whereas 10 kΩ results in lower static power dissipation.

2.24.2 ROM Based Straps

If ROM is attached (see ROMIDCFG pin based straps), then after RSTb goes inactive (high), the ROM is read at the addresses listed below to default to the internal settings.

Table 2-25 ROM Based Straps

Strap	ROM location	Description	ASIC default if no ROM
AGPVCOGAIN(2:0)	Byte 0x70, Bits 2:0	AGP PLL VCO gain control. iPVG(2:0) on the macro If not ROM, then default taken from the bonding options and register settings	Bit 2:1 from the bonding options, bit 0 from the register default
AGPCPGAIN(2:0)	Byte 0x70, Bits 6:4	AGP PLL charge pump gain control. iPCP(2:0) on the macro If not ROM, then default taken from the bonding options and register settings	Bit 2:1 from the bonding options, bit 0 from the register default
APAD_STRENGTH3_3V	Byte 0x71	Controls default impedance of AGP/PCI pads for PCI, AGP 1x and AGP 2 x (3.3V environment) Bits 7:4 N-MOS impedance control Bits 3:0 P-MOS impedance control	PCI: 0xF5 AGP 3.3V: 0x77
APAD_STRENGTH1_5V	Byte 0x72	Controls default impedance of AGP/PCI pads for AGP 4 x (1.5V environment) Bits 7:4 N-MOS impedance control Bits 3:0 P-MOS impedance control	AGP 1.5V: 0x8E
CHG_ID	Byte 0x73, Bit 0	CHG_ID: 0 No ROM, ID = **LY** or (0x4C59) 1 No ROM, ID = **LZ** or (0x4C5A) If no ROM attached, see ROMIDCFG pin based straps.	ROMIDCFG pin based straps CHG_ID = 0, not populated, internal pull-down or ROM based strap. CHG_ID = 1, external pull-up or ROM based strap.
AP_SIZE(1:0)	Byte 0x73, Bits 5:4	Size of the primary memory aperture (frame buffer) claimed in PCI configuration space. 00 = 128 MB 01 = 256 MB 10 = 64 MB 11 = reserved	00
SUBSYS_VEN_ID(15:0)	Byte 0x74- 0x75	Sub-System Vendor ID (SSVID) for PCI configuration space. If no ROM attached, then for motherboard system ROM writes in the SSVID **before** the enumeration cycle is initiated, else for dual-chip card, slave chip uses 0x1002 as SSVID.	1002h (i.e. ATI) Note: should not be 0 if no ROM

Table 2-25 ROM Based Straps (Continued)

Strap	ROM location	Description	ASIC default if no ROM
SUBSYS_ID(15:0)	Byte 0x76- 0x77	Sub-System ID (SSID) for PCI configuration space. If no ROM attached, then for motherboard system ROM writes in the SSID **before** the enumeration cycle is initiated, else for dual-chip card, slave chip uses DEVICE_ID as SSID.	Same as DEVICE_ID. See CHG_ID. Note: should not be 0 if no ROM

2.24.3 Strap Latching and Wake-Up Procedure

This section is intended to provide an outline of the M6 internal reset and strap latching sequence. For more details.

Table 2-26 Strap Latching and Wake-up

Time	Event	Actions
T1	RSTb input from PCI/AGP goes active (low)	All chip output pins tri-state
T2 (T1 + ?)	PCICLK starts running	
T3 (T2 + 3 PCICLKs)	Internal resets go active	All internal clocks start running at PCICLK speed. AGP PLL is bypassed (no phase locking). All internal registers go to their default values.
T4	RSTb goes inactive (high)	All pin based straps are latched. If ROM is attached, reads start to get ROM based strap data.
T5	If ROM attached, then ROM reads for strap data complete. If no ROM, then T5 and T4 have the same value.	Remove reset from AGP PLL and allow it to start locking. Start PLL lock counter.
T6 *	PLL lock counter finished. Takes 2^13=8192 PCICLK's.	Switch internal BCLK from bypass to locked AGP PLL output (if BUSCFG mode where PLL clk is used). Start reset counter.
T7 (T6 + 8 PCICLKs)	Reset counter done.	All internal resets go inactive.
T8 (T7 + 4 PCICLKs)	Chip ready for PCI/AGP configuration cycles.	

* If the BUSCFG pin based strap settings are such that the AGP PLL clock is not used (e.g. PCI 33), step T6 above is shortened to no time.

2.24.4 Readback of Strap Settings

All straps can be read back from internal registers so that software may examine them. The table below lists the location of all these register fields.

Table 2-27 Strap Setting Readback

Strap	Read	Write	Default
VGA_DISABLE	CONFIG_XSTRAP(0)	No write	From pin
BUSCFG(2:0)	CONFIG_XSTRAP(26:24)	No write	From pins
AGPSKEW(1:0)	CONFIG_XSTRAP(7:6)	No write	From pins
X1CLK_SKEW(1:0)	CONFIG_XSTRAP(9:8)	No write	From pins
ROMIDCFG(2:0)	CONFIG_XSTRAP(22:20)	No write	From pins
ID_DISABLE	CONFIG_XSTRAP(14)	No write	From pin
AP_SIZE(1:0)	CONFIG_XSTRAP(17:16)	No write	ROM: from ROM No ROM: “00”
CHG_ID(1:0)	Read indirectly by looking at the DEVICE_ID	No write	ROM: from ROM No ROM: from GPIO(11) pin
SUBSYS_VEN_ID(15:0)	PCICFG 0x2C-0x2D	PCICFG 0x4C-0x4D	ROM: from ROM No ROM: 0x1002
SUBSYS_ID(15:0)	PCICFG 0x2E-0x2F	PCICFG 0x4E-0x4F	ROM: from ROM No ROM: DEVICE_ID
APD_STRENGTH	PAD_CTLR_STRENGTH	Use PAD_MANUAL_OVERRIDE function	ROM: from ROM No ROM PCI: 0xF5 No ROM AGP 1x/2x: 0x77 No ROM AGP 4x: 0x8E
AGPVCOGAIN(2:1)	APLL_VCO_GAIN(2:1)	Can write	ROM; from the ROM No ROM: from the bonding pins
AGPVCOGAIN(0)	APLL_VCO_GAIN(0)	Can write	1
AGPCPGAIN(2:1)	APLL_PUMP_GAIN(2:1)	Can write	ROM; from the ROM No ROM: from the bonding pins
AGPCPGAIN(0)	APLL_PUMP_GAIN(0)	Can write	0

Chapter 3
Physical Dimensions

3.1 M6 Physical Dimensions

Package Outline: BGA 35mm x 35mm - 484 (420 + 64) pins

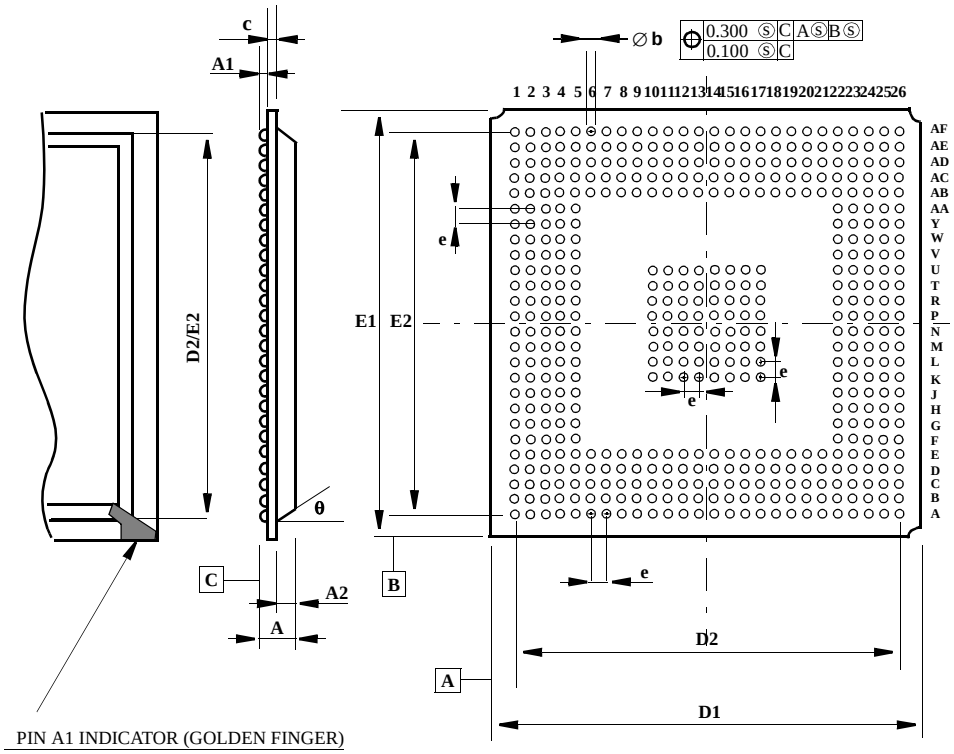

Figure 3-1. Physical Dimensions of M6

Table 3-1 484-Pin BGA Package Physical Dimensions

Ref	Min	Normal	Max
c	0.51	0.56	0.61
A	2.20	2.33	2.50
A1	-	0,60	-
A2	1.12	1.17	1.22
ϕb	-	0.75	-
D1	34.80	35	35.20
D2	29.80	30.00	30.20
E1	34.80	35	35.20
E2	29.80	30.00	30.20
F1	-	31.75	-
F2	-	31.75	-
e	-	1.27	-
ddd	-	-	0.15
θ	-	30 deg typ	-

Appendix A
Pin Listings

This appendix shows the pin listings for M6 family members. To go to the listing of interest, use the following list of linked cross references:

"M6 Pin List Sorted by Ball Reference" on page A-2

"M6 Pin List Sorted by Signal Name" on page A-10

A.1 M6 Pin List Sorted by Ball Reference

Table A-1 Signals Listed by Ball Reference

Ball Ref	Signal Name	Ball Ref	Signal Name
A1	VSS	B15	DQ(24)
A10	A(11)	B16	DQ(23)
A11	A(8)	B17	DQ(19)
A12	A(4)	B18	DQ(16)
A13	A(1)	B19	QS(1)
A14	DQ(29)	B2	VSS
A15	DQ(25)	B20	DQ(13)
A16	DQMb(2)	B21	DQ(9)
A17	DQ(20)	B22	DQ(7)
A18	DQ(17)	B23	DQ(4)
A19	QS(0)	B24	VDDQM
A2	MPVDD	B25	DQ(1)
A20	DQ(14)	B26	AGPREF
A21	DQ(10)	B3	CLKFB
A22	DQMb(0)	B4	CLK1b
A23	DQ(5)	B5	CLK1b_IN
A24	DQ(3)	B6	CLK0b
A25	DQ(2)	B7	CLK0b_IN
A26	DQ(0)	B8	CSb(1)
A3	MPVSS	B9	CSb(0)
A4	CLK1	C1	DQ(33)
A5	CLK1_IN	C10	A(9)
A6	CLK0	C11	A(6)
A7	CLK0_IN	C12	A(2)
A8	CKE	C13	DQ(31)
A9	RASb	C14	DQ(27)
B1	DQ(32)	C15	DQMb(3)
B10	A(10)	C16	DQ(22)
B11	A(7)	C17	DQ(18)
B12	A(3)	C18	QS(3)
B13	A(0)	C19	DQ(15)
B14	DQ(28)	C2	DQ(34)

Table A-1 Signals Listed by Ball Reference

Ball Ref	Signal Name	Ball Ref	Signal Name
C20	DQ(12)	D4	VSS
C21	DQ(8)	D5	VSS
C22	DQ(6)	D6	VDDQM
C23	VDDM	D7	VDDRH
C24	VDDQM	D8	WEb
C25	AGPTEST	D9	A(12)
C26	AD(1)	E1	DQ(37)
C3	VSS	E10	VDDC
C4	VSS	E11	VDDR1
C5	VDDQM	E12	VDDC
C6	VDDQM	E13	VDDR1
C7	VDDM	E14	VDDR1
C8	CASb	E15	VDDC
C9	A(13)	E16	VDDR1
D1	DQ(35)	E17	VDDC
D10	VDDM	E18	VDDR1
D11	A(5)	E19	VDDC
D12	VDDM	E2	DQ(38)
D13	DQ(30)	E20	VDDR1
D14	DQ(26)	E21	VDDR1
D15	VDDQM	E22	VDDP
D16	DQ(21)	E23	AD(4)
D17	VDDM	E24	AD(6)
D18	QS(2)	E25	AD(5)
D19	VDDQM	E26	AD(7)
D2	DQ(36)	E3	VDDM
D20	DQ(11)	E4	VSS
D21	DQMb(1)	E5	VSS
D22	VDDQM	E6	VDDR1
D23	VDDM	E7	VDDR1
D24	AD(0)	E8	VDDC
D25	AD(2)	E9	VDDR1
D26	AD(3)	F1	DQ(39)
D3	VSS	F2	DQMb(4)

Table A-1 Signals Listed by Ball Reference

Ball Ref	Signal Name	Ball Ref	Signal Name
F22	VDDP	J26	DEVSELb
F23	CBEb(0)	J3	DQ(47)
F24	AD_STBb(0)	J4	QS(4)
F25	AD_STB(0)	J5	VDDR1
F26	AD(8)	K1	QS(5)
F3	VDDQM	K10	VSS
F4	VDDM	K11	VSS
F5	VSS	K12	VSS
G1	DQMb(5)	K13	VSS
G2	DQ(40)	K14	VSS
G22	VDDP	K15	VSS
G23	AD(9)	K16	VSS
G24	AD(11)	K17	VSS
G25	AD(10)	K2	QS(6)
G26	AD(12)	K22	VDDC
G3	DQ(41)	K23	VDDP
G4	VDDQM	K24	TRDYb
G5	VDDR1	K25	FRAMEb
H1	DQ(42)	K26	IRDYb
H2	DQ(43)	K3	QS(7)
H22	VDDC	K4	VDDR1
H23	VDDP	K5	VDDC
H24	AD(13)	L1	DQ(48)
H25	AD(15)	L10	VSS
H26	AD(14)	L11	VSS
H3	DQ(44)	L12	VSS
H4	VDDR1	L13	VSS
H5	VDDC	L14	VSS
J1	DQ(45)	L15	VSS
J2	DQ(46)	L16	VSS
J22	VDDP	L17	VSS
J23	PAR	L2	DQ(49)
J24	STOPb	L22	VDDP
J25	CBEb(1)	L23	AD(16)

Table A-1 Signals Listed by Ball Reference

Ball Ref	Signal Name	Ball Ref	Signal Name
L24	AD(18)	N22	VDDP
L25	CBEb(2)	N23	CBEb(3)
L26	AD(17)	N24	AD_STBb(1)
L3	DQ(50)	N25	AD(21)
L4	DQ(51)	N26	AD(23)
L5	VDDR1	N3	DQMb(7)
M1	DQ(52)	N4	DQ(56)
M10	VSS	N5	VDDR1
M11	VSS	P1	DQ(57)
M12	VSS	P10	VSS
M13	VSS	P11	VSS
M14	VSS	P12	VSS
M15	VSS	P13	VSS
M16	VSS	P14	VSS
M17	VSS	P15	VSS
M2	DQ(53)	P16	VSS
M22	VDDC	P17	VSS
M23	VDDP	P2	DQ(58)
M24	AD(20)	P22	VDDP
M25	AD(22)	P23	AD(24)
M26	AD(19)	P24	AD(26)
M3	DQ(54)	P25	AD_STB(1)
M4	VDDR1	P26	AD(25)
M5	VDDC	P3	DQ(59)
N1	DQ(55)	P4	DQ(60)
N10	VSS	P5	VDDR1
N11	VSS	R1	DQ(61)
N12	VSS	R10	VSS
N13	VSS	R11	VSS
N14	VSS	R12	VSS
N15	VSS	R13	VSS
N16	VSS	R14	VSS
N17	VSS	R15	VSS
N2	DQMb(6)	R16	VSS

Table A-1 Signals Listed by Ball Reference

Ball Ref	Signal Name	Ball Ref	Signal Name
R17	VSS	U15	VSS
R2	DQ(62)	U16	VSS
R22	VDDC	U17	VSS
R23	VDDP	U2	GPIO(10)
R24	AD(28)	U22	VDDC
R25	AD(27)	U23	VDDP
R26	AD(29)	U24	SBA(5)
R3	DQ(63)	U25	SB_STBb
R4	VDDR1	U26	SBA(4)
R5	VDDC	U3	GPIO(9)
T1	MEMVMODE	U4	VDDR3
T10	VSS	U5	VDDC
T11	VSS	V1	GPIO(8)
T12	VSS	V2	GPIO(7)
T13	VSS	V22	VDDP
T14	VSS	V23	SBA(3)
T15	VSS	V24	SBA(1)
T16	VSS	V25	SB_STB
T17	VSS	V26	SBA(2)
T2	VREF	V3	GPIO(6)
T22	VDDP	V4	GPIO(5)
T23	AD(30)	V5	VDDR3
T24	SBA(7)	W1	GPIO(4)
T25	AD(31)	W2	GPIO(3)
T26	SBA(6)	W22	VDDC
T3	GPIO(13)	W23	VDDP
T4	GPIO(12)	W24	SERRb
T5	VDDR3	W25	SBA(0)
U1	GPIO(11)	W26	RBFb
U10	VSS	W3	GPIO(2)
U11	VSS	W4	VDDR3
U12	VSS	W5	VDDC
U13	VSS	Y1	GPIO(1)
U14	VSS	Y2	GPIO(0)

Table A-1 Signals Listed by Ball Reference

Ball Ref	Signal Name	Ball Ref	Signal Name
Y22	VDDP	AB24	VDDP
Y23	ST(1)	AB25	STP_AGPb
Y24	GNTb	AB26	AGP_BUSYb
Y25	ST(2)	AB3	ZV_LCDDATA(3)
Y26	ST(0)	AB4	ZV_LCDDATA(4)
Y3	ROMCSb	AB5	VDDR3
Y4	ZV_LCDCNTL(0)	AB6	VDDR3
Y5	VDDR3	AB7	VDDC
AA1	ZV_LCDCNTL(1)	AB8	VDDC
AA2	ZV_LCDCNTL(2)	AB9	BLONb
AA22	VDDP	AC1	ZV_LCDDATA(5)
AA23	RSTb	AC10	TXOUT_L3N
AA24	INTAb	AC11	TXOUT_U1N
AA25	REQb	AC12	TXCLK_UN
AA26	PCICLK	AC13	LVDDR
AA3	ZV_LCDCNTL(3)	AC14	CRT2DDCDAT
AA4	ZV_LCDDATA(0)	AC15	A2VSSN
AA5	VDDR3	AC16	A2VSSN
AB1	ZV_LCDDATA(1)	AC17	VDDR3
AB10	VDDR3	AC18	TXVSSR
AB11	DIGON	AC19	TXVDDR
AB12	VDDC	AC2	ZV_LCDDATA(6)
AB13	CRT2DDCCLK	AC20	DVIDDCDATA
AB14	VDDC	AC21	AVSSQ
AB15	VDDR3	AC22	AUXWIN
AB16	VDDR3	AC23	VDDR3
AB17	VDDC	AC24	VDDR3
AB18	VDDR3	AC25	VGADDCCLK
AB19	VDDC	AC26	VGADDCDATA
AB2	ZV_LCDDATA(2)	AC3	ZV_LCDDATA(7)
AB20	VDDR3	AC4	VDDR3
AB21	VDDR3	AC5	ZV_LCDDATA(23)
AB22	VDDR3	AC6	TESTEN
AB23	VDDP	AC7	LTGIO(2)

Table A-1 Signals Listed by Ball Reference

Ball Ref	Signal Name	Ball Ref	Signal Name
AC8	TXOUT_L0N	AE15	LVSSR
AC9	TXOUT_L1N	AE16	R2SET
AD1	ZV_LCDDATA(8)	AE17	TXVSSR
AD10	TXOUT_L3P	AE18	TXCM
AD11	TXOUT_U1P	AE19	TX0M
AD12	TXCLK_UP	AE2	ZV_LCDDATA(12)
AD13	LVDDR	AE20	TX1M
AD14	H2SYNC	AE21	TX2M
AD15	A2VSSQ	AE22	RSET
AD16	A2VDDQ	AE23	VSYNC
AD17	A2VDD	AE24	HSYNC
AD18	TXVSSR	AE25	STEREOSYNC
AD19	TXVDDR	AE26	PVDD
AD2	ZV_LCDDATA(9)	AE3	ZV_LCDDATA(16)
AD20	DVIDDCCLK	AE4	ZV_LCDDATA(18)
AD21	HPD	AE5	ZV_LCDDATA(21)
AD22	AVSSN	AE6	SSIN
AD23	AVDD	AE7	SSOUT
AD24	MONID(0)	AE8	TXOUT_L2N
AD25	MONID(1)	AE9	TXCLK_LN
AD26	PVSS	AF1	ZV_LCDDATA(13)
AD3	ZV_LCDDATA(10)	AF10	TXOUT_U0N
AD4	ZV_LCDDATA(19)	AF11	TXOUT_U2N
AD5	ZV_LCDDATA(22)	AF12	TXOUT_U3P
AD6	LTGIO(1)	AF13	COMP_B
AD7	LTGIO(0)	AF14	Y_G
AD8	TXOUT_L0P	AF15	C_R
AD9	TXOUT_L1P	AF16	TPVSS
AE1	ZV_LCDDATA(11)	AF17	TPVDD
AE10	TXOUT_U0P	AF18	TXCP
AE11	TXOUT_U2P	AF19	TX0P
AE12	TXOUT_U3N	AF2	ZV_LCDDATA(14)
AE13	V2SYNC	AF20	TX1P
AE14	LVSSR	AF21	TX2P

Table A-1 Signals Listed by Ball Reference

Ball Ref	Signal Name	Ball Ref	Signal Name
AF22	B		
AF23	G		
AF24	R		
AF25	XTALIN		
AF26	XTALOUT		
AF3	ZV_LCDDATA(15)		
AF4	ZV_LCDDATA(17)		
AF5	ZV_LCDDATA(20)		
AF6	LPVSS		
AF7	LPVDD		
AF8	TXOUT_L2P		
AF9	TXCLK_LP		

A.2 M6 Pin List Sorted by Signal Name

Table A-2 Pins Listed by Signal Name

Signal Name	Ball Ref	Signal Name	Ball Ref
A(0)	B13	AD(20)	M24
A(1)	A13	AD(21)	N25
A(10)	B10	AD(22)	M25
A(11)	A10	AD(23)	N26
A(12)	D9	AD(24)	P23
A(13)	C9	AD(25)	P26
A(2)	C12	AD(26)	P24
A(3)	B12	AD(27)	R25
A(4)	A12	AD(28)	R24
A(5)	D11	AD(29)	R26
A(6)	C11	AD(3)	D26
A(7)	B11	AD(30)	T23
A(8)	A11	AD(31)	T25
A(9)	C10	AD(4)	E23
A2VDD	AD17	AD(5)	E25
A2VDDQ	AD16	AD(6)	E24
A2VSSN	AC15	AD(7)	E26
A2VSSN	AC16	AD(8)	F26
A2VSSQ	AD15	AD(9)	G23
AD(0)	D24	AD_STB(0)	F25
AD(1)	C26	AD_STB(1)	P25
AD(10)	G25	AD_STBb(0)	F24
AD(11)	G24	AD_STBb(1)	N24
AD(12)	G26	AGP_BUSYb	AB26
AD(13)	H24	AGPREF	B26
AD(14)	H26	AGPTEST	C25
AD(15)	H25	AUXWIN	AC22
AD(16)	L23	AVDD	AD23
AD(17)	L26	AVSSN	AD22
AD(18)	L24	AVSSQ	AC21
AD(19)	M26	B	AF22
AD(2)	D25	BLONb	AB9

Table A-2 Pins Listed by Signal Name

Signal Name	Ball Ref	Signal Name	Ball Ref
C_R	AF15	DQ(19)	B17
CASb	C8	DQ(2)	A25
CBEb(0)	F23	DQ(20)	A17
CBEb(1)	J25	DQ(21)	D16
CBEb(2)	L25	DQ(22)	C16
CBEb(3)	N23	DQ(23)	B16
CKE	A8	DQ(24)	B15
CLK0	A6	DQ(25)	A15
CLK0_IN	A7	DQ(26)	D14
CLK0b	B6	DQ(27)	C14
CLK0b_IN	B7	DQ(28)	B14
CLK1	A4	DQ(29)	A14
CLK1_IN	A5	DQ(3)	A24
CLK1b	B4	DQ(30)	D13
CLK1b_IN	B5	DQ(31)	C13
CLKFB	B3	DQ(32)	B1
COMP_B	AF13	DQ(33)	C1
CRT2DDCCLK	AB13	DQ(34)	C2
CRT2DDCDAT	AC14	DQ(35)	D1
CSb(0)	B9	DQ(36)	D2
CSb(1)	B8	DQ(37)	E1
DEVSELb	J26	DQ(38)	E2
DIGON	AB11	DQ(39)	F1
DQ(0)	A26	DQ(4)	B23
DQ(1)	B25	DQ(40)	G2
DQ(10)	A21	DQ(41)	G3
DQ(11)	D20	DQ(42)	H1
DQ(12)	C20	DQ(43)	H2
DQ(13)	B20	DQ(44)	H3
DQ(14)	A20	DQ(45)	J1
DQ(15)	C19	DQ(46)	J2
DQ(16)	B18	DQ(47)	J3
DQ(17)	A18	DQ(48)	L1
DQ(18)	C17	DQ(49)	L2

Table A-2 Pins Listed by Signal Name

Signal Name	Ball Ref	Signal Name	Ball Ref
DQ(5)	A23	GPIO(10)	U2
DQ(50)	L3	GPIO(11)	U1
DQ(51)	L4	GPIO(12)	T4
DQ(52)	M1	GPIO(13)	T3
DQ(53)	M2	GPIO(2)	W3
DQ(54)	M3	GPIO(3)	W2
DQ(55)	N1	GPIO(4)	W1
DQ(56)	N4	GPIO(5)	V4
DQ(57)	P1	GPIO(6)	V3
DQ(58)	P2	GPIO(7)	V2
DQ(59)	P3	GPIO(8)	V1
DQ(6)	C22	GPIO(9)	U3
DQ(60)	P4	H2SYNC	AD14
DQ(61)	R1	HPD	AD21
DQ(62)	R2	HSYNC	AE24
DQ(63)	R3	INTAb	AA24
DQ(7)	B22	IRDYb	K26
DQ(8)	C21	LPVDD	AF7
DQ(9)	B21	LPVSS	AF6
DQMb(0)	A22	LTGIO(0)	AD7
DQMb(1)	D21	LTGIO(1)	AD6
DQMb(2)	A16	LTGIO(2)	AC7
DQMb(3)	C15	LVDDR	AC13
DQMb(4)	F2	LVDDR	AD13
DQMb(5)	G1	LVSSR	AE14
DQMb(6)	N2	LVSSR	AE15
DQMb(7)	N3	MEMVMODE	T1
DVIDDCCLK	AD20	MONID(0)	AD24
DVIDDCDATA	AC20	MONID(1)	AD25
FRAMEb	K25	MPVDD	A2
G	AF23	MPVSS	A3
GNTb	Y24	PAR	J23
GPIO(0)	Y2	PCICLK	AA26
GPIO(1)	Y1	PVDD	AE26

Table A-2 Pins Listed by Signal Name

Signal Name	Ball Ref	Signal Name	Ball Ref
PVSS	AD26	STOPb	J24
QS(0)	A19	STP_AGPb	AB25
QS(1)	B19	TESTEN	AC6
QS(2)	D18	TPVDD	AF17
QS(3)	C18	TPVSS	AF16
QS(4)	J4	TRDYb	K24
QS(5)	K1	TX0M	AE19
QS(6)	K2	TX0P	AF19
QS(7)	K3	TX1M	AE20
R	AF24	TX1P	AF20
R2SET	AE16	TX2M	AE21
RASb	A9	TX2P	AF21
RBFb	W26	TXCLK_LN	AE9
REQb	AA25	TXCLK_LP	AF9
ROMCSb	Y3	TXCLK_UN	AC12
RSET	AE22	TXCLK_UP	AD12
RSTb	AA23	TXCM	AE18
SB_STB	V25	TXCP	AF18
SB_STBb	U25	TXOUT_L0N	AC8
SBA(0)	W25	TXOUT_L0P	AD8
SBA(1)	V24	TXOUT_L1N	AC9
SBA(2)	V26	TXOUT_L1P	AD9
SBA(3)	V23	TXOUT_L2N	AE8
SBA(4)	U26	TXOUT_L2P	AF8
SBA(5)	U24	TXOUT_L3N	AC10
SBA(6)	T26	TXOUT_L3P	AD10
SBA(7)	T24	TXOUT_U0N	AF10
SERRb	W24	TXOUT_U0P	AE10
SSIN	AE6	TXOUT_U1N	AC11
SSOUT	AE7	TXOUT_U1P	AD11
ST(0)	Y26	TXOUT_U2N	AF11
ST(1)	Y23	TXOUT_U2P	AE11
ST(2)	Y25	TXOUT_U3N	AE12
STEREOSYNC	AE25	TXOUT_U3P	AF12

Table A-2 Pins Listed by Signal Name

Signal Name	Ball Ref	Signal Name	Ball Ref
TXVDDR	AC19	VDDM	D17
TXVDDR	AD19	VDDM	D23
TXVSSR	AC18	VDDM	E3
TXVSSR	AD18	VDDM	F4
TXVSSR	AE17	VDDP	AA22
V2SYNC	AE13	VDDP	AB23
VDDC	AB12	VDDP	AB24
VDDC	AB14	VDDP	E22
VDDC	AB17	VDDP	F22
VDDC	AB19	VDDP	G22
VDDC	AB7	VDDP	H23
VDDC	AB8	VDDP	J22
VDDC	E10	VDDP	K23
VDDC	E12	VDDP	L22
VDDC	E15	VDDP	M23
VDDC	E17	VDDP	N22
VDDC	E19	VDDP	P22
VDDC	E8	VDDP	R23
VDDC	H22	VDDP	T22
VDDC	H5	VDDP	U23
VDDC	K22	VDDP	V22
VDDC	K5	VDDP	W23
VDDC	M22	VDDP	Y22
VDDC	M5	VDDQM	B24
VDDC	R22	VDDQM	C24
VDDC	R5	VDDQM	C5
VDDC	U22	VDDQM	C6
VDDC	U5	VDDQM	D15
VDDC	W22	VDDQM	D19
VDDC	W5	VDDQM	D22
VDDM	C23	VDDQM	D6
VDDM	C7	VDDQM	F3
VDDM	D10	VDDQM	G4
VDDM	D12	VDDR1	E11

Table A-2 Pins Listed by Signal Name

Signal Name	Ball Ref	Signal Name	Ball Ref
VDDR1	E13	VDDR3	V5
VDDR1	E14	VDDR3	W4
VDDR1	E16	VDDR3	Y5
VDDR1	E18	VDDRH	D7
VDDR1	E20	VGADDCCLK	AC25
VDDR1	E21	VGADDCDATA	AC26
VDDR1	E6	VREF	T2
VDDR1	E7	VSS	A1
VDDR1	E9	VSS	B2
VDDR1	G5	VSS	C3
VDDR1	H4	VSS	C4
VDDR1	J5	VSS	D3
VDDR1	K4	VSS	D4
VDDR1	L5	VSS	D5
VDDR1	M4	VSS	E4
VDDR1	N5	VSS	E5
VDDR1	P5	VSS	F5
VDDR1	R4	VSS	K10
VDDR3	AA5	VSS	K11
VDDR3	AB10	VSS	K12
VDDR3	AB15	VSS	K13
VDDR3	AB16	VSS	K14
VDDR3	AB18	VSS	K15
VDDR3	AB20	VSS	K16
VDDR3	AB21	VSS	K17
VDDR3	AB22	VSS	L10
VDDR3	AB5	VSS	L11
VDDR3	AB6	VSS	L12
VDDR3	AC17	VSS	L13
VDDR3	AC23	VSS	L14
VDDR3	AC24	VSS	L15
VDDR3	AC4	VSS	L16
VDDR3	T5	VSS	L17
VDDR3	U4	VSS	M10

Table A-2 Pins Listed by Signal Name

Signal Name	Ball Ref	Signal Name	Ball Ref
VSS	M11	VSS	T13
VSS	M12	VSS	T14
VSS	M13	VSS	T15
VSS	M14	VSS	T16
VSS	M15	VSS	T17
VSS	M16	VSS	U10
VSS	M17	VSS	U11
VSS	N10	VSS	U12
VSS	N11	VSS	U13
VSS	N12	VSS	U14
VSS	N13	VSS	U15
VSS	N14	VSS	U16
VSS	N15	VSS	U17
VSS	N16	VSYNC	AE23
VSS	N17	WEb	D8
VSS	P10	XTALIN	AF25
VSS	P11	XTALOUT	AF26
VSS	P12	Y_G	AF14
VSS	P13	ZV_LCDCNTL(0)	Y4
VSS	P14	ZV_LCDCNTL(1)	AA1
VSS	P15	ZV_LCDCNTL(2)	AA2
VSS	P16	ZV_LCDCNTL(3)	AA3
VSS	P17	ZV_LCDDATA(0)	AA4
VSS	R10	ZV_LCDDATA(1)	AB1
VSS	R11	ZV_LCDDATA(10)	AD3
VSS	R12	ZV_LCDDATA(11)	AE1
VSS	R13	ZV_LCDDATA(12)	AE2
VSS	R14	ZV_LCDDATA(13)	AF1
VSS	R15	ZV_LCDDATA(14)	AF2
VSS	R16	ZV_LCDDATA(15)	AF3
VSS	R17	ZV_LCDDATA(16)	AE3
VSS	T10	ZV_LCDDATA(17)	AF4
VSS	T11	ZV_LCDDATA(18)	AE4
VSS	T12	ZV_LCDDATA(19)	AD4

Table A-2 Pins Listed by Signal Name

Signal Name	Ball Ref	Signal Name	Ball Ref
ZV_LCDDATA(2)	AB2		
ZV_LCDDATA(20)	AF5		
ZV_LCDDATA(21)	AE5		
ZV_LCDDATA(22)	AD5		
ZV_LCDDATA(23)	AC5		
ZV_LCDDATA(3)	AB3		
ZV_LCDDATA(4)	AB4		
ZV_LCDDATA(5)	AC1		
ZV_LCDDATA(6)	AC2		
ZV_LCDDATA(7)	AC3		
ZV_LCDDATA(8)	AD1		
ZV_LCDDATA(9)	AD2		

This page intentionally left blank.