Developer Note

Power Macintosh Computers

Power Macintosh 6100/60
Power Macintosh 6100/60AV
Power Macintosh 7100/66
Power Macintosh 7100/66AV
Power Macintosh 8100/80
Power Macintosh 8100/80AV

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About This Developer Note

This developer note introduces the Power Macintosh family, Apple Computer's first Macintosh computers that use the PowerPC microprocessor. It is written primarily for experienced Macintosh hardware and software developers who want to create products that are compatible with these computers.

The discussion assumes that you are already familiar with the general technology of Macintosh computers. If you are unfamiliar with Macintosh technology or would like more technical information, you may want to obtain copies of the related technical documents listed in "Supplementary Documents," later in this preface.

This note is published in two forms: an online version included with the Apple Developer CD and a looseleaf paper version published by APDA. For information about APDA, see "Supplementary Documents," later in this preface.

Contents of This Note

This developer note is divided into four chapters:

- Chapter 1, "Introduction," presents an overview of the features of Power Macintosh computers, the configurations in which they are offered, and the differences between them and other Macintosh computers.
- Chapter 2, "Hardware Overview," describes the Power Macintosh circuit boards, including their functional units, signal timing, memory management, and other general characteristics.
- Chapter 3, "Input and Output Interfaces," describes the interfaces of Power Macintosh computers with peripheral equipment, including details of signal handling, connectors, and pin assignments.
- Chapter 4, "Expansion Capabilities," contains interface specifications for plug-in expansion cards compatible with Power Macintosh computers, with details of card configuration and pin assignments.

Two appendixes follow the main part of this note:

- Appendix A, "Overview of PowerPC Technology," gives some of the background of the PowerPC RISC microprocessor and tells how it differs from CISC processors such as the Motorola MC68040 and the Intel processors.
- Appendix B, "Power Macintosh Application Development," summarizes the process of developing application software to run on Power Macintosh computers. More detailed information is given in *Inside Macintosh: PowerPC System Software* and *Building Programs for PowerPC Processor–Based Macintosh Computers*. These books are listed in "Supplementary Documents," later in this preface.

At the end of this developer note are a glossary and an index.

Supplementary Documents

The following documents provide information that complements or extends the information in this developer note.

Apple Publications

Inside Macintosh is a collection of books, organized by topic, that describe the system software of Macintosh computers. Together, these books provide the essential reference for programmers, software designers, and engineers. Current volumes include the following titles:

Inside Macintosh: Overview
Inside Macintosh: Macintosh Toolbox Essentials
Inside Macintosh: More Macintosh Toolbox
Inside Macintosh: Files
Inside Macintosh: Processes
Inside Macintosh: Memory
Inside Macintosh: Operating System Utilities
Inside Macintosh: Imaging With QuickDraw
Inside Macintosh: Text
Inside Macintosh: Interapplication Communication
Inside Macintosh: Devices
Inside Macintosh: QuickTime
Inside Macintosh: QuickTime Components
Inside Macintosh: Networking

Inside Macintosh: PowerPC System Software covers in detail the changes and extensions to Macintosh system software version 7.1 for Power Macintosh computers, including the run-time architecture and new Macintosh Toolbox managers.

Building Programs for PowerPC Processor–Based Macintosh Computers is a general discussion for developers of the development and building of application software for PowerPC processor–based Macintosh systems, including Power Macintosh computers.

Technical Introduction to the Macintosh Family, second edition, surveys the complete Macintosh family of computers from the developer's point of view.

Macintosh Human Interface Guidelines provides authoritative information on the theory behind the Macintosh "look and feel" and Apple's standard ways of using individual interface components.

Making It Macintosh is an interactive guide to human-computer interface design for Macintosh software. This CD-ROM disc contains more than 100 animated examples that demonstrate the correct use of Macintosh human interface elements.

Designing Cards and Drivers for the Macintosh Family, third edition, explains the hardware and software requirements for drivers and NuBus™ '90 expansion cards compatible with Macintosh computers, including the Power Macintosh computers covered by this developer note.

Technical Note 144 (*Macintosh Color Monitor Connections*) and Technical Note 326 (*M.HW.SenseLines*) provide technical details of the interfaces to various Apple and third-party monitors.

The *NuBus Block Transfers* technical note provides information about block data transfers to and from NuBus expansion cards.

Macintosh Developer Note Number 5 contains both hardware and system software details for the Macintosh Quadra 840AV and Macintosh Centris 660AV computers, which feature the Apple AV technologies.

Macintosh Developer Note Number 8 includes *Macintosh DAV Interface for NuBus Expansion Cards,* a developer note that describes how expansion cards can access digital audio-video data in Power Macintosh AV computers.

The Apple publications listed above are available from APDA. APDA is Apple's worldwide source for over three hundred development tools, technical resources, training products, and information for anyone interested in developing applications on Apple platforms. Customers receive the quarterly *APDA Tools Catalog* featuring all current versions of Apple development tools and the most popular third-party development tools. Ordering is easy; there are no membership fees, and application forms are not required for most products. APDA offers convenient payment and shipping options, including site licensing.

To order products or to request a complimentary copy of the *APDA Tools Catalog,* contact

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Other Publications

The following documents are available from the organizations listed:

Comité Consultatif International Radio (CCIR):

Recommended Standard 601-2

Institute for Electrical and Electronics Engineers (IEEE):

Standard 1196

IT&T:

ASCO 2300 Audio-Stereo Codec Specification

Motorola:

PowerPC 601 RISC Microprocessor User's Manual

Conventions and Abbreviations

This developer note uses the following typographical conventions and abbreviations.

Typographical Conventions

New terms appear in **boldface** where they are first defined.

Computer-language text—any text that is literally the same as it appears in computer input or output—appears in `Courier` font.

Hexadecimal numbers are preceded by a dollar sign ($). For example, the hexadecimal equivalent of decimal 16 is written as $10.

Note
A note like this contains information that is interesting but not essential for an understanding of the text. ◆

IMPORTANT
A note like this contains important information that you should read before proceeding. ▲

▲ **WARNING**
A note like this directs your attention to something that could cause damage or result in a loss of data. ▲

Standard Abbreviations

Abbreviations for standard units of measure used in this developer note include

A	amperes	MHz	megahertz
cm	centimeters	mm	millimeters
dB	decibels	ms	milliseconds
GB	gigabytes	mV	millivolts
Hz	Hertz	ns	nanoseconds
KB	kilobytes	pF	picofarads
Kbit	kilobits	sec.	seconds
kHz	kilohertz	V	volts
kΩ	kilohms	µF	microfarads
mA	milliamperes	µsec	microseconds
MB	megabytes	Ω	ohms
Mbit	megabits		

Other abbreviations used in this developer note include

AC	alternating current
ADB	Apple Desktop Bus
ADC	analog-to-digital converter
AGND	analog ground
AMIC	Apple Memory-Mapped Input/Output Controller
API	application programming interface
ASIC	application-specific integrated circuit
AWAC	audio waveform amplifier and converter
CAS	column address strobe
CCIR	Comité Consultatif International Radio
CD-ROM	compact disc read-only memory
CISC	complex instruction set computing
CIVIC	Cyclone Integrated Video Interfaces Controller
CLUT	color lookup table
CMOS	complementary metal-oxide semiconductor
CPU	central processing unit
DAC	digital-to-analog converter
DC	direct current
DMA	direct memory access
DP	data path
DRAM	dynamic random-access memory

EMI	electromagnetic interference
FIFO	first-in, first-out
GCR	Group Code Recording
GND	ground
HMC	high-speed memory controller
HPV	high-performance video
IEEE	Institute of Electrical and Electronics Engineers
I/O	input/output
ISDN	Integrated Services Digital Network
MACE	Media Access Controller for Ethernet
MFM	Modified Frequency Modulation
MMU	memory management unit
n.a.	not applicable
NC	no connection
PAL	Phased Alternate Lines
PBX	Private Branch Exchange
PDS	processor-direct slot
RAM	random-access memory
RAS	row address strobe
RGB	red-green-blue
RISC	reduced instruction set computing
rms	root mean square
ROM	read-only memory
SCC	Serial Communications Controller
SCSI	Small Computer System Interface
SIMM	Single Inline Memory Module
SNR	signal-to-noise ratio
VCR	videocassette recorder
VIA	Versatile Interface Adapter
VRAM	video random-access memory

CHAPTER 1

Introduction

Power Macintosh 6100/60, 6100/60AV, 7100/66, 7100/66AV, 8100/80, and 8100/80AV computers represent the first generation of products in Apple Computer's transition to reduced instruction set computing (RISC), using the PowerPC 601 microprocessor. RISC technology increases computing speed dramatically. Even the low end of the Power Macintosh family, the competitively priced Power Macintosh 6100/60, delivers more than twice the performance of any previous Macintosh computer.

This chapter describes the first generation of Power Macintosh computers in general terms and lists some of their features and differences. For a discussion of Apple's RISC technology in general, see Appendix A, "Overview of PowerPC Technology."

The First Generation of Power Macintosh

The first generation of Power Macintosh computers consists of three fast, powerful desktop models with nearly identical electronic circuitry. Their principal differences are their processor speeds and mechanical configurations:

- The Power Macintosh 6100/60 and 6100/60AV run at 60 MHz and are housed in a low-profile enclosure designed to be placed under the user's monitor. In physical form they resemble the Macintosh Quadra 610 and Macintosh Centris 660AV.
- The Power Macintosh 7100/66 and 7100/66AV run at 66 MHz and are housed in a mid-size enclosure similar to that of the Macintosh II and Macintosh Quadra 650.
- The Power Macintosh 8100/80 and 8100/80AV run at 80 MHz and are housed in a minitower enclosure, like that of the Macintosh Quadra 800 and 840AV. The minitower design provides more room for internal disk drives and expansion cards.

The Power Macintosh model designations ending in AV are configurations that support the video capture and output features of the Apple AV Technologies.

Principal hardware features of the Power Macintosh 6100/60, 7100/66, and 8100/80 include

- a PowerPC 601 RISC microprocessor
- built-in video output for standard monitors
- provision for NuBus™ and processor-direct expansion cards
- built-in Ethernet support
- built-in GeoPort support, compatible with most telephone systems
- high-quality 16-bit stereo sound input and output
- a wide range of RAM, disk drive, and CD-ROM configurations

Besides these capabilities, the Power Macintosh 6100/60AV, 7100/66AV, and 8100/80AV provide sophisticated video I/O processing facilities. These and other features are discussed further in "Features and Capabilities," later in this chapter. Chapter 2, "Hardware Overview," provides more detailed hardware information. For a summary of Power Macintosh software, see Appendix B, "Power Macintosh Application Development."

Models and Configurations

Power Macintosh computers have many common features. They differ mainly in physical form, speed, and expansion facilities:

- The Power Macintosh 6100/60 and 6100/60AV, the least expensive models in the family, are housed in a low-profile enclosure similar to that of the Macintosh Quadra 610 and Centris 660AV. They run at 60 MHz and have one processor-direct slot (PDS) for an expansion card. To add NuBus capability to the Power Macintosh 6100/60, the user installs the Power Macintosh 6100 NuBus™ adapter card. The Power Macintosh 6100/60 is shipped with its expansion slot empty; the Power Macintosh 6100/60AV is shipped with an AV card installed. Both models have built-in support for a variety of monitors, including Apple AudioVision displays. The Power Macintosh 6100 NuBus adapter card and AV card are described in "Apple Expansion Cards," later in this chapter.
- The Power Macintosh 7100/66 and 7100/66AV are housed in a full-sized desktop configuration similar to that of the Macintosh IIvx and Macintosh Quadra 650. They run at 66 MHz and have three NuBus slots for expansion cards plus a separate processor-direct slot (PDS) for extending their video capabilities. Besides built-in display support, the Power Macintosh 7100/66 is shipped with a VRAM expansion card installed and the Power Macintosh 7100/66AV is shipped with an AV card installed.
- The Power Macintosh 8100/80 and 8100/80AV are housed in a minitower configuration similar to that of the Macintosh Quadra 800 and 840AV. They run at 80 MHz and have three NuBus slots for expansion cards plus a separate PDS for extending their video capabilities. Besides built-in display support, the Power Macintosh 8100/80 is shipped with a VRAM expansion card installed and the Power Macintosh 8100/80AV is shipped with an AV card installed. Both models are shipped with second-level cache memory installed.

For details of the monitor and video I/O support provided by various Power Macintosh models, see "Audio and Video Features," later in this chapter.

Disk Storage and RAM

All Power Macintosh computers include a new version of the Apple SuperDrive floppy disk drive that conforms to common industry practice by not including the automatic disk injection feature of previous versions of the Apple SuperDrive. It is capable of accepting floppy disks up to 1.44 MB capacity.

The user can add a variety of external disk drives to any Power Macintosh computer by using the external SCSI port. For details of the possible SCSI configurations, see "SCSI Connection," in Chapter 3.

The specific shipping configurations for the first generation of Power Macintosh computers are listed in Table 1-1 on page 4. Bundled expansion cards are described in "Apple Expansion Cards," later in this chapter.

Table 1-1 Configurations of Power Macintosh computers

Catalog number	RAM size	Hard disk drive size	Built-in CD-ROM	Bundled PDS expansion card
Power Macintosh 6100/60 models:				
M2196LL / A	8 MB	160 MB	No	None
M2197LL / A	8 MB	160 MB	Yes	None
M1878LL / A	8 MB	250 MB	Yes	None
Power Macintosh 6100/60AV model:				
M2738LL / A	8 MB	250 MB	Yes	AV
Power Macintosh 7100/66 models:				
M2464LL / A	8 MB	250 MB	No	VRAM expansion
M2465LL / A	8 MB	250 MB	Yes	VRAM expansion
M2466LL / A	8 MB	500 MB	Yes	VRAM expansion
Power Macintosh 7100/66AV model:				
M2467LL / A	8 MB	500 MB	Yes	AV
Power Macintosh 8100/80 models:				
M1884LL / A	8 MB	250 MB	No	VRAM expansion
M2199LL / A	16 MB	500 MB	No	VRAM expansion
M2284LL / A	16 MB	500 MB	Yes	VRAM expansion
M2294LL / A	16 MB	1 GB	No	VRAM expansion
Power Macintosh 8100/80AV model:				
M2293LL / A	16 MB	500 MB	Yes	AV

The user can expand the RAM capacity of any Power Macintosh computer by installing Single Inline Memory Module (SIMM) cards. Including RAM expansion, there are a wide range of options for expanding and reconfiguring computers of the Power Macintosh family. Some important options are summarized in Table 1-2.

All Power Macintosh models support secondary cache expansion to 256 KB; this expansion is standard with the Power Macintosh 8100/80 and 8100/80AV.

RAM SIMMs must be installed in pairs. Possible RAM configurations in Power Macintosh computers are shown in Table 4-6 on page 57.

For more detailed information about user expansion of Power Macintosh computers, see Chapter 4, “Expansion Capabilities.”

Audio and Video Features

All Power Macintosh models contain built-in support for Apple displays, using main RAM for frame buffering. This support drives monitors up to 13 inches in size at color

Table 1-2 Expansion capabilities

	Power Macintosh model		
System feature	6100/60	7100/66	8100/80
Maximum RAM capacity	72 MB	136 MB	264 MB
Maximum number of internal SCSI devices	2	2	3
Room for a 1-GB internal SCSI drive	No	No	Yes
NuBus slots	1*	3	3
Maximum VRAM capacity	None†	2 MB	4 MB

* Using the optional NuBus adapter card
† 2 MB with the optional AV card installed

depths up to 16 bits and monitors up to 16 inches in size at color depths up to 8 bits. The built-in display connection is described in "Built-in Interface for Video Monitors," in Chapter 3.

The Power Macintosh 7100/66 and 8100/80 models are shipped with VRAM expansion cards installed in their PDS slots. These cards provide a second monitor output in addition to the computer's built-in display support. The user can expand the VRAM capacity of these cards to drive monitors up to 21 inches at color depths up to 24 bits. The VRAM expansion cards are described in the next section.

All Power Macintosh models also feature built-in high-quality stereo sound input and output capabilities. These capabilities, which support speech recognition and synthesis as well as broadcast-quality 16-bit sound, are described in "Sound I/O," in Chapter 3.

For a description of Apple's system software support for speech recognition and synthesis, see *Macintosh Developer Note Number 5*. This book is described in "Supplementary Documents," in the preface.

Three Power Macintosh models also include the video input and output features of the Apple AV Technologies. These model are designated Power Macintosh 6100/60AV, 7100/66AV, and 8100/80AV. They contain an Apple AV card, instead of a VRAM expansion card, in their PDS slots. The Power Macintosh 7100/66AV and 8100/80AV models still accept NuBus cards; the Power Macintosh 6100/60AV cannot have a NuBus capability because its single PDS slot is occupied by the AV card. A connector on the AV card lets NuBus cards in the Power Macintosh 7100/66AV and 8100/80AV access audio and video signals directly by means of a card-to-card ribbon cable. This connector is described in "DAV Interface," in Chapter 4. AV capabilities are described in the next section; for more detailed technical information, see "AV Card," in Chapter 3.

The Power Macintosh 6100/60AV, 7100/66AV, and 8100/80AV models are shipped with built-in CD-ROM drives to support their multimedia capabilities.

Table 1-3 summarizes the VRAM capacities for second monitors in Power Macintosh computers, in addition to AudioVision display support. Table 1-3 also shows which

models can accept video input and deliver video output, using the VRAM provided for the second monitor.

Table 1-3 VRAM capacities and video I/O support

Power Macintosh model	VRAM size (MB)	Video I/O support
6100/60	None	No
6100/60AV	2	Yes
7100/66, standard VRAM	1	No
7100/66, extended VRAM	2	No
7100/66AV	2	Yes
8100/80, standard VRAM	2	No
8100/80, extended VRAM	4	No
8100/80AV	2	Yes

For more information about VRAM expansion, see “VRAM Expansion SIMMs,” in Chapter 4. The various VRAM frame buffer sizes shown in Table 1-3 can support monitors up to 21 inches at color depths up to 24 bits, as shown in Table 1-4.

Table 1-4 Monitors supported by various VRAM sizes

Buffer size (MB)	Monitors supported
1	Up to 14-inch size at up to 16 bits, up to 16-inch size at up to 8 bits
2	Up to 16-inch size at up to 24 bits, up to 21-inch size at up to 16 bits
4	Up to 21-inch size at up to 24 bits

Apple Expansion Cards

Apple supplies four plug-in cards for the processor-direct slot of Power Macintosh computers:

- The Power Macintosh 6100 NuBus adapter card gives the Power Macintosh 6100/60 a NuBus expansion capability. The adapter card contains the BART NuBus controller chip that is included on the main logic board of the other Power Macintosh models. It plugs into the PDS slot of the Power Macintosh 6100/60 and accepts one short (7-inch) NuBus card, which lies parallel to the main logic board. This arrangement is shown in Figure 4-1, on page 53.
- The Power Macintosh 7100 VRAM expansion card adds a second monitor output and 1 MB of 32-bit video random-access memory (VRAM) separate from system RAM. The monitor output is a DB-15 connector, described in "VRAM Expansion Cards," in Chapter 3. The user can expand the VRAM capacity to 2 MB by installing four VRAM SIMM cards. These SIMM cards are described in "VRAM Expansion SIMMs," in Chapter 4.
- The Power Macintosh 8100 VRAM expansion card acts the same as the Power Macintosh 7100 VRAM expansion card, described above, but it has 2 MB of VRAM and is expandable to 4 MB. It lets the Power Macintosh 8100/80 support 21-inch monitors to a color depth of 16 bits (using 2 MB of VRAM) or 24 bits (using 4 MB of VRAM).
- The **AV card** adds 2 MB of VRAM to the Power Macintosh 6100/60AV, 7100/66AV, and 8100/80AV, while extending the computer's capabilities to include the video I/O features of the Apple AV Technologies—all the video input and output features of the Macintosh Quadra 840AV and Macintosh Centris 660AV, including compatibility with NTSC, PAL, and SECAM television signals. The AV card is equipped with S-video input and output connectors as well as a DB-15 monitor connector. The user can connect the AV card to standard television equipment by means of adapter cables for composite video that are included with the computer. These video capabilities and their I/O connections are separate from the AudioVision display interface that comes with the computer.

IMPORTANT

The Power Macintosh 6100 NuBus adapter card is sold separately to users who want to add a NuBus capability to the Power Macintosh 6100/60. The VRAM expansion cards and the AV card are bundled with the specific computer models shown in Table 1-1; at present they are not available separately, and the computers are not sold without the cards. ▲

Note

The Power Macintosh 7100 VRAM card and the Power Macintosh 8100 VRAM card use different SIMMs to expand their VRAM capacities. For further information, see "VRAM Expansion SIMMs," in Chapter 4. ◆

I/O Accessories

Apple offers the following I/O hardware accessories for all Power Macintosh models:

- An analog telecom adapter that plugs into the Apple GeoPort connector and communicates with a variety of telephone systems.
- An Ethernet cable adapter that plugs into the Ethernet connector.
- An adapter cable for users who want to connect a monitor that is not an AudioVision display to the built-in monitor connector. This cable has an AudioVision HDI-45 plug at one end and a DB-15 monitor socket at the other end.
- Adapter cables that plug into input and output connectors of the AV card and provide composite video, using connectors compatible with standard television equipment. These cables are included with all models that contain the AV card.
- A special microphone, optimized for speech recognition, that plugs into the audio input connector.

Features and Capabilities

Besides standard features common to Macintosh technology, Power Macintosh computers have these new or improved capabilities:

- *Direct memory access.* A high-speed memory controller (HMC) and an Apple Memory-Mapped I/O Controller (AMIC) provide direct memory access (DMA) between main memory and peripheral devices. DMA permits very fast transfers of large amounts of data without burdening the main processor.
- *Widely compatible video input.* Models with the AV card installed can process composite or S-video inputs in NTSC, PAL, and SECAM formats from external sources such as videocams and videocassette recorders (VCRs), using standard television-type connectors. The AV card stores video information in RGB form in a frame buffer separate from main memory.
- *Flexible video output.* All models have a built-in capacity to support monitors up to 16-inch size. VRAM expansion cards give the Power Macintosh 7100/66 and 8100/80 a separate ability to support a second monitor up to 21-inch size. Models with the AV card installed (that is, those designated AV) can also exchange NTSC and PAL composite and S-video signals with other kinds of video equipment, including television sets and VCRs, besides driving a monitor. The AV card supports color depths up to 24 bits for graphics and 16 bits for video on a separate monitor up to 21 inches in size.
- *Improved NuBus interface.* All models use the BART NuBus controller for NuBus expansion cards. This chip is described in “Functional Units—Main Circuit Board,” in Chapter 2. It supports NuBus block transfers and data bursts to and from the main processor bus. NuBus capability is optional in the Power Macintosh 6100/60 and is not available in the Power Macintosh 6100/60AV.

- *Widely compatible floppy disk drive.* The 1.44 MB manual-inject floppy disk drive supports both Apple's Group Code Recording (GCR) format and DOS-compatible Modified Frequency Modulation (MFM) format.
- *Built-in Ethernet support.* All models contain built-in circuitry for Ethernet I/O.
- *Enhanced serial ports.* Two serial ports both support RS-232 and RS-422 serial I/O protocols, as well as AppleTalk I/O over LocalTalk networks.
- *Integrated telephone I/O.* All models provide Apple's high-performance serial I/O capability (called GeoPort) on two serial ports, permitting connection to analog, PBX, ISDN, facsimile (fax), and data telephone lines. GeoPort supports full-duplex telephone I/O at transmission rates up to 9600 bits per second.
- *Enhanced sound I/O.* All models provide 16-bit digital stereo sound I/O at sample rates up to 44.1 kHz. Sound generated by the system can be mixed with CD-ROM sound in analog form.
- *Large-capacity ROM.* ROM chips totaling 4 MB are provided with all models. These chips contain some of the system software that is on the hard disk in other Apple computers. They are mounted on SIMM cards, so the user can replace them if an upgrade becomes available in the future.
- *Expansion slots.* The Power Macintosh 7100/66, 7100/66AV, 8100/80, and 8100/80AV contain three NuBus slots for long or short Macintosh expansion cards; the Power Macintosh 6100/60 accepts one short card using an optional angle adapter card. All slots carry a 32-bit data and address bus. The NuBus slots in the Power Macintosh 7100/66, 7100/66AV, 8100/80, and 8100/80AV exist in addition to the PDS slot that supports a video expansion card.
- *Mass media support.* All models support up to a total of seven SCSI devices. Within this limit, the user can connect several external devices to any model's SCSI port in addition to removable internal hard disk drives and CD-ROM drives.
- *Fast SCSI support.* The Power Macintosh 8100/80 and 8100/80AV provide a fast SCSI interface (up to 10 MB per second) for internal SCSI devices, in addition to the standard SCSI interface.
- *Software on/off power control.* The Power Macintosh 7100/66 and 8100/80 provide power control service to their NuBus expansion slots, so expansion cards can turn the computer on and off.
- *Replaceable real-time clock battery.* The real-time clock and parameter RAM in all models are powered by a long-life plug-in battery.
- *Automatic SCSI termination.* Built-in circuitry provides automatic termination of the internal and external SCSI cables if no SCSI devices are connected.

Apple offers Power Macintosh computers, together with their I/O accessories and expansion cards, in all domestic and international markets for Apple computers. Units sold outside the United States are correctly localized for the regions in which they are marketed.

Machine Identification

By using the Gestalt Manager with the identifier `gestaltMachineType`, an application or expansion card firmware can determine the model type of the user's system. Power Macintosh computers also set the 3 low bits of the 32-bit register at address $5FFF FFFC to a machine identification code. Table 1-5 lists the gestalt and register values that identify each basic model of the Power Macintosh family.

Table 1-5 CPU identification

Model	Gestalt value	Register value
Power Macintosh 6100/60 and 6100/60AV	$4B	000
Power Macintosh 7100/66 and 7100/66AV	$70	010
Power Macintosh 8100/80 and 8100/80AV	$41	011

CHAPTER 2

Hardware Overview

Power Macintosh computers are shipped with built-in floppy disk drives and removable internal hard disk drives. For each model, the addition of an external monitor, a keyboard, and a mouse forms a complete personal computing system.

This chapter provides a more detailed description of the memory and processing hardware common to all Power Macintosh models. For details of I/O hardware, see Chapter 3, "Input and Output Interfaces." For information about PowerPC processor operation and software, see Appendix A, "Overview of PowerPC Technology," and Appendix B, "Power Macintosh Application Development."

Physical Forms

Power Macintosh computers are generally described in "Models and Configurations," in Chapter 1. The external dimensions of their enclosures are shown in Table 2-1.

Table 2-1 External dimensions

	Power Macintosh model		
Dimension	6100/60 and 6100/60AV	7100/66 and 7100/66AV	8100/80 and 8100/80AV
Width	16.3 inches (41.4 cm)	13.0 inches (33.0 cm)	7.8 inches (19.7 cm)
Depth	14.8 inches (37.6 cm)	16.6 inches (42.2 cm)	16.0 inches (40.6 cm)
Height	3.2 inches (8.1 cm)	6.0 inches (15.2 cm)	14.3 inches (36.2 cm)

All models contain essentially the same circuitry and system components, with variations as noted in the next section.

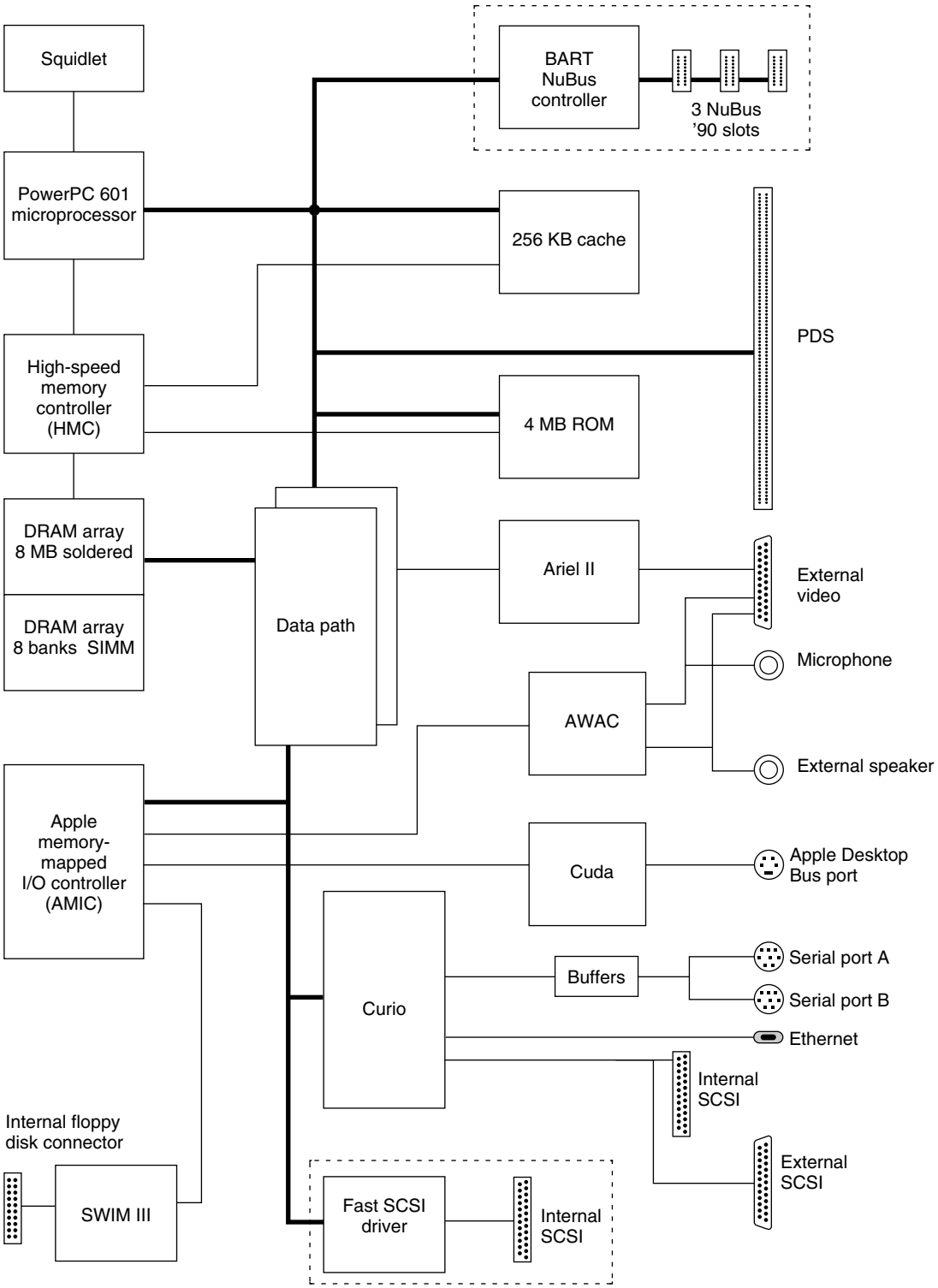
System Architecture

The overall data flow relations among the hardware units of Power Macintosh models 6100/60, 7100/66, and 8100/80 are summarized by the block diagram in Figure 2-1, which shows the circuitry of the Power Macintosh 8100/80. Certain parts are omitted from the main circuit board in the Power Macintosh 6100/60 and 7100/66; these parts are enclosed in dotted lines in Figure 2-1:

- In the Power Macintosh 6100/60, the BART NuBus controller and a single NuBus slot connector are mounted on a plug-in NuBus adapter card.
- In the Power Macintosh 6100/60, 6100/60AV, 7100/66, and 7100/66AV, the fast internal SCSI bus is omitted.

The units shown in Figure 2-1 are described in the next section. Components of the AV card that is bundled with the Power Macintosh 6100/60AV, 7100/66AV, and 8100/80AV are described in "Functional Units—AV Card," later in this chapter.

Figure 2-1 Block diagram for Power Macintosh 8100/80



Functional Units—Main Circuit Board

All circuitry shown in Figure 2-1 is contained on a single multilayer circuit board, which bears markings that identify each chip. Features of the major integrated circuit chips are summarized in the next sections.

Main Processor

The main processor in Power Macintosh 6100/60, 7100/66, and 8100/80 computers is a PowerPC 601 microprocessor. Its operational theory is summarized in Appendix A, "Overview of PowerPC Technology." The principal features of the PowerPC 601 microprocessor include

- full RISC processing architecture
- parallel integer and floating-point processing units
- a branch manager that can usually implement branches by reloading the incoming instruction queue without using any processing time
- an internal memory management unit (MMU)
- 32 Kbit of on-chip cache memory

For complete technical details, see the Motorola *PowerPC 601 RISC Microprocessor User's Manual.* This book is listed in "Supplementary Documents," in the preface.

Read-Only Memory

Power Macintosh computers contain 4 MB of ROM with 100-ns access time. Some of the system software that was on disk in previous Macintosh computers is in ROM in Power Macintosh models.

Random-Access Memory

RAM for Power Macintosh computers is provided by dynamic random-access memory (DRAM) chips, of which the first 8 MB of RAM capacity is soldered to the main logic board. Users may expand RAM capacity by adding 72-pin Single Inline Memory Modules (SIMMs) in pairs. Each SIMM contains two banks of DRAM with up to 16 MB of capacity per bank. The maximum RAM capacity of each Power Macintosh model is given in Table 1-2 on page 5.

For further information about RAM SIMMs, see "RAM Expansion SIMMs," in Chapter 4. RAM addressing and RAM access details are discussed in "Memory Management," later in this chapter.

Cache Memory

The PowerPC 601 microprocessor maintains a 32-Kbit internal first-level cache. For details of its organization and operation, see the Motorola *PowerPC 601 RISC Microprocessor User's Manual.* This book is listed in "Supplementary Documents," in the preface.

All Power Macintosh models accept an external second-level cache on a SIMM. The second-level cache size may range from 128 KB to 256 KB. The Power Macintosh 8100/80 is shipped with all 256 KB already installed; users of other models in the Power Macintosh family can install a second-level cache by plugging a SIMM into a 160-pin connector on the main logic board. The high-speed memory controller (HMC) interrogates two pins of this connector during system startup, to determine the size of the memory on the SIMM. If no SIMM is installed, pull-up resistors on these pins cause the HMC to disable all external cache operations. The HMC is described in the next section.

For pin assignments and mechanical details of the cache SIMM, see "Cache Expansion SIMMs," in Chapter 4.

High-Speed Memory Controller

The **high-speed memory controller (HMC)** is an ASIC chip that controls all memory operations in Power Macintosh computers. The HMC has the following features that support data transfers to and from the PowerPC 601 processor:

- support for all basic transfer protocols, including all single-cycle accesses
- support for four-cycle 32-byte cache accesses
- translation of misaligned read actions into double-word read actions
- implementation of address-only transactions
- bus arbitration (of the address bus only) as described in "CPU Bus Arbitration," later in this chapter.

The HMC does not support the following features:

- pipelining of memory bus transactions
- cache snooping
- recovery from transfer error acknowledge signals
- little-endian transfer mode (see "Data Organization," in Appendix A)

Apple Memory-Mapped I/O Controller

The **Apple Memory-Mapped I/O Controller (AMIC)** is a 160-pin gate array chip that performs most I/O logic and control for Power Macintosh computers. It supports the following functions:

- handling interrupts received through Versatile Interface Adapter (VIA) channels
- DMA for Ethernet I/O

- DMA for the SWIM III floppy disk drive controller
- DMA for the Serial Communications Controller (SCC) I/O
- DMA for Small Computer System Interface (SCSI) device support
- DMA for sound I/O
- monitor support

The AMIC does not support the extended transfer protocols of the PowerPC 601 processor; using these protocols will cause a transfer error exception.

Data Path Chips

Two data path (DP) chips provide buffering between I/O and DRAM memory accesses and the cached CPU bus. They perform the following functions:

- route byte lanes between 8-bit and 16-bit I/O processes and the 64-bit CPU bus
- provide first-in, first-out (FIFO) buffering for video monitor data, which is fetched from RAM as eight-cycle bursts
- supply the Ariel II video chip with appropriate timing signals for video monitor data

The Ariel II video chip is described in the next section.

Ariel II Video Chip

The **Ariel II** video chip provides a color lookup table (CLUT) and digital-to-analog converter (DAC) for driving an AudioVision monitor. For information about monitors compatible with Power Macintosh computers, see “Built-in Interface for Video Monitors,” in Chapter 3.

SWIM III Floppy Disk Drive Controller

The **SWIM III** floppy disk drive controller is an extension of the SWIM II circuitry used in models such as the Macintosh Quadra 800 and Macintosh Centris 650. It includes the following new features:

- support for DMA data transfers, which minimize use of the main processor
- no requirement that interrupts be disabled during floppy disk accesses
- support for GCR and MFM formats on 1.44 MB disks
- compatibility with the manual-inject floppy disk drive

Floppy disk drives designed to be compatible with the New Age controller used in the Macintosh Quadra 840AV and Macintosh Centris 660AV computers can easily be adapted for compatibility with the SWIM III controller.

Curio I/O Chip

The **Curio** is a multipurpose I/O chip that contains a Media Access Controller for Ethernet (MACE), a SCSI controller, and a Serial Communications Controller (SCC).

The SCC section of the Curio includes 8-byte FIFO buffers for both transmit and receive data streams.

Curio functions are discussed in "External Device Interfaces," in Chapter 3.

Cuda Microcontroller Chip

The **Cuda** is a microcontroller chip. It

- turns system power on and off
- manages system resets from various commands
- maintains parameter RAM
- manages the Apple Desktop Bus (ADB)
- manages the real-time clock
- lets an external signal from either Apple GeoPort serial port control system power

The ADB is discussed in more detail in "Apple Desktop Bus," in Chapter 3; Apple GeoPort is discussed in "Serial Ports," in the same chapter.

AWAC Sound Chip

The **audio waveform amplifier and converter (AWAC)** is a 44-pin chip that combines a waveform amplifier with a 16-bit digital sound encoder and decoder (codec). It conforms to the IT&T *ASCO 2300 Audio-Stereo Codec Specification* (listed in "Supplementary Documents," in the preface) and furnishes high-quality sound I/O for Power Macintosh computers. For details of AWAC operation, see "Sound I/O," in Chapter 3.

BART NuBus Controller

The **BART NuBus controller** chip provides the data gateway between NuBus and the CPU bus. It acts as a CPU bus master, transferring one-cycle or four-cycle transactions. It is compliant with the IEEE Standard 1196 listed in "Supplementary Documents," in the preface. For further information about NuBus in Power Macintosh computers, see "NuBus Interface," in Chapter 4, and the Macintosh Hardware Technical Notes.

Squidlet Chip

Squidlet is a 28-pin chip that provides a set of synchronized system clocks for Power Macintosh computers. Clock frequencies are listed in "System Clocks," later in this chapter.

Functional Units—AV Card

The AV card, described in “Apple Expansion Cards,” in Chapter 1, is bundled with the Power Macintosh 6100/60AV, 7100/66AV, and 8100/80AV. Features of the major chips on the AV card are summarized in the next sections. For details of their operation, see “AV Card,” in Chapter 3.

Cyclone Integrated Video Interfaces Controller

The **Cyclone Integrated Video Interfaces Controller (CIVIC),** used in the AV card, is a CMOS chip in a 144-pin package. The CIVIC

- manages from 1 MB to 4 MB of video RAM (VRAM)
- controls data transfers between VRAM and the SAA7194 chip and between VRAM and the Sebastian video color palette chip (both chips are described later in this chapter)
- provides 32-bit or 64-bit data paths between VRAM and the main processor; supports data bursts from the main processor in all transfer modes
- controls convolution of graphics data for line-interlaced displays
- provides NTSC and PAL timing signals
- generates vertical blanking and video-in interrupt signals

Sebastian Chip

The **Sebastian** chip is a video color palette and video digital-to-analog converter (DAC) in a 100-pin CMOS configuration, used in the AV card. The Sebastian

- accepts digital data up to 64 bits wide, either as one 64-bit port or as one or two 32-bit ports
- lets one 32-bit port handle digital video while the other processes graphics (including QuickTime), using the same or different color lookup tables
- supports mixing video with still graphics, even with different color depths
- supports both Truecolor and pseudocolor with alpha color lookup
- supports a transparency effect when blending video with still graphics under the control of alpha channel bits at 1 to 8 bits per pixel
- uses a convolution filter to minimize flicker in line-interlaced displays
- supports displays with dot clocks up to 100 MHz

SAA7194 Decoder

The SAA7194 is a Philips CMOS chip that decodes the color information in NTSC, PAL, and SECAM video formats using a clock synchronized to their line frequency. It is used in the AV card. The SAA7194 also

- performs input video window scaling with horizontal and vertical filtering
- produces 16-bit 1:5:5:5 RGB, 8-bit grayscale, or YUV 4:2:2 output

For details of SAA7194 operation, see “AV Card,” in Chapter 3.

Mickey Encoder

The **Mickey** is a composite video encoder in a 28-pin advanced bipolar CMOS chip. It is used in the AV card. The Mickey

- accepts analog RGB video signals from the Sebastian video color palette chip
- encodes to NTSC or PAL format
- produces S-video, composite, or RGB video outputs

System Clocks

The Power Macintosh circuitry is driven by several different clocks running at different frequencies. Clocks that run at different rates in different models include the system clock, which is controlled by an oscillator and drives the PowerPC processor, and the CPU bus clock, which is controlled by the system clock. The frequencies of these clocks are listed in Table 2-2.

Table 2-2 Model-specific clocks

Power Macintosh models	System clock frequency (MHz)	CPU bus clock frequency (MHz)
6100/60 and 6100/60AV	60.0000	30.0000
7100/66 and 7100/66AV	66.0000	33.0000
8100/80 and 8100/80AV	80.0000	40.0000

Clocks that run at the same rate in the Power Macintosh 6100/60, 6100/60AV, 7100/66, 7100/66AV, 8100/80, and 8100/80AV are listed in Table 2-3.

Table 2-3 Fixed-rate system clocks

Name	Frequency (MHz)	Source	Use
I/O	31.3344	Oscillator	I/O components, 12-inch monitor, SCC
VGA	25.1570	Oscillator	VGA monitor
Dot	57.2832	Oscillator	16-inch monitor
Ethernet	20.0000	Oscillator	Ethernet, SCSI
Cuda	0.0320	Crystal	Cuda real-time clock
Sound	44.1584	Oscillator	Sound sample rate

CPU Bus

The CPU bus is the standard 64-bit nonpipelined bus used by the PowerPC 601 processor. Expansion cards can connect to the CPU bus through the processor-direct slot (PDS) connector, described in "PDS Expansion Cards for the Power Macintosh 6100/60," in Chapter 4.

CPU Bus Arbitration

The HMC performs arbitration of the address part of the CPU bus in the order shown in Table 2-4, with the processor having default access. Access to the data part of the CPU bus is dependent on access to the address part.

Table 2-4 CPU bus arbitration order

Priority	Requestor
Highest	DRAM refresh
	Video refresh
	I/O DMA for SWIM III
	I/O DMA for AWAC
	I/O DMA for SCSI
	I/O DMA for SCC
	Expansion card
Lowest	Main processor

An expansion card can assert control of the CPU bus, subject to these design considerations:

- The requesting card must verify that the bus is free by checking signal ABB (pin 125).
- Original access to the bus is delayed by a latency period of one CPU clock cycle.
- Only basic processor cycles and cache line operations are recognized.
- A slave expansion card must decode its own memory space and must ensure that it does not interfere with the computer's main memory usage.
- Higher-priority bus grants may interfere with a card's access to the bus; in particular, video refresh actions may sometimes absorb much of the bus capacity.

Address Errors

The main processor's memory management unit (MMU) normally maps only address spaces that are decoded in hardware. Attempts to access undecoded addresses result in an MMU error, which is recoverable.

If an attempt is made to access an address that is mapped by the MMU but not decoded in hardware, the AMIC chip asserts an error signal after 40 µs. This error condition is not generally recoverable; it forces the user to restart the computer.

Memory Management

All memory operations are controlled by the HMC chip, described in "High-Speed Memory Controller," earlier in this chapter.

Memory Organization

Memory in Power Macintosh computers is organized in three levels:

- internal cache memory in the main processor
- external second-level cache memory
- DRAM memory

The internal cache memory capacity is 32 Kbits. The user can expand external secondary cache capacity up to 256 KB. The limits to RAM capacity for various models are given in Table 1-2 on page 5.

Details of physical memory space access are given in the next section.

Physical Memory Allocations

A single 32-bit physical memory space contains the memory allocations shown in Table 2-5. Virtual memory operations are supported by the internal memory management unit of the PowerPC 601 microprocessor. Logical memory mapping is established by the system software.

Table 2-5 Physical memory allocations

Range	Used for
$0000 0000–$0FFF FFFF	RAM
$1000 0000–$3FFF FFFF	RAM aliases
$4000 0000–$4FFF FFFF	ROM
$5000 0000–$5FFF FFFF	I/O
$6000 0000–$FEFF FFFF	Not assigned
$FF00 0000–$FFFF FFFF	ROM alias

RAM Access

All Power Macintosh models use 80-ns dynamic RAM chips. The RAM system supports the PowerPC 601 four-cycle bus transaction and all PowerPC 601 single-cycle bus transactions. It does not support any of the PowerPC 601 extended protocol bus transactions.

Note
Transactions where the CPU bus is master have the lowest priority among RAM access requests. For further information, see "CPU Bus Arbitration," earlier in this chapter. ◆

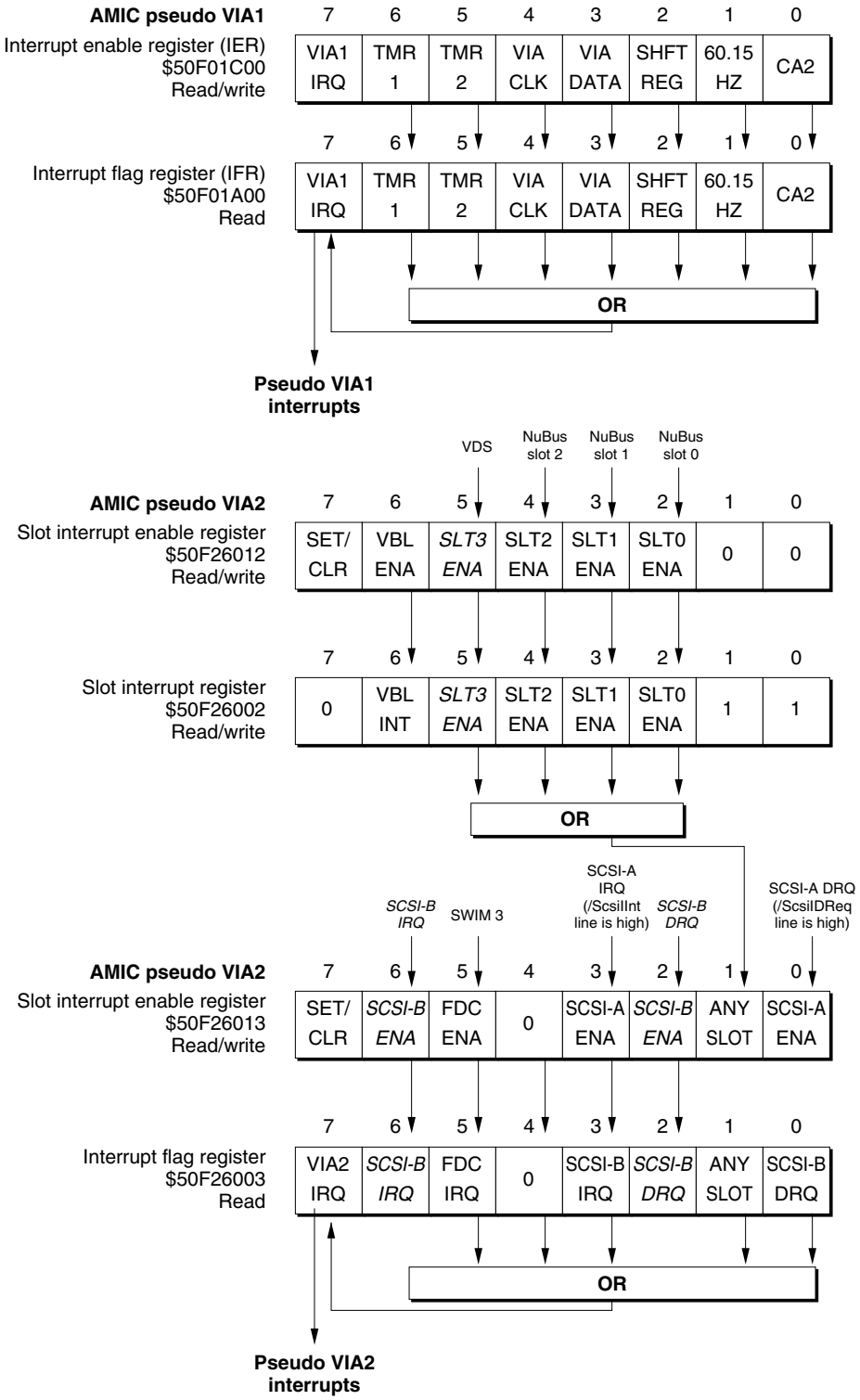
DRAM refresh takes place as a CAS before RAS memory cycle every 15.6 µsec. This cycle does not affect RAM timing for data accesses.

Interrupt Handling

Traditional Macintosh software is designed for the seven-level interrupt structure of the Motorola MC68000 family of processors. The PowerPC 601 processor, however, has only a single interrupt line and service routine. The AMIC chip resolves this difference by emulating the MC68000 interrupt structure and accepting interrupts through the traditional VIA channels. The process of handling VIA1 and VIA2 interrupts in the Power Macintosh 7100/66, 7100/66AV, 8100/80, and 8100/80AV is diagrammed in Figure 2-2. Elements not present in the Power Macintosh 6100/60 and 6100/60AV are labeled in *italics.*

For further information about interrupt handling through the VIA channels, see *Inside Macintosh: Processes.*

Figure 2-2 Emulated interrupt handling



CHAPTER 3

Input and Output Interfaces

Power Macintosh computers are offered with two levels of I/O capability:

- Models without an AV designation after the model name provide the I/O features that are currently standard for Macintosh Quadra computers: ADB, GeoPort, SCSI, a floppy disk drive, built-in Ethernet, high-quality 16-bit stereo sound, and various levels of monitor support up to 21 inches, depending on the model.
- Models with an AV designation (the Power Macintosh 6100/60AV, 7100/66AV, and 8100/80AV) provide the full range of Apple AV Technologies in addition to the standard I/O features; they add video input and output, as well as support for 21-inch monitors.

This chapter provides details of the Power Macintosh I/O hardware and interfaces. For a list of Power Macintosh configurations, see Table 1-1 on page 4.

External Device Interfaces

This section discusses the interfaces between Power Macintosh computers and external devices through

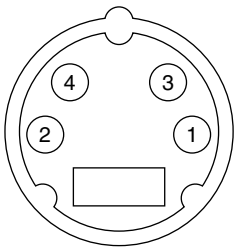
- the ADB, which supports keyboards, mouse devices, trackballs, and other user-input devices
- an Ethernet port for wide area network access
- two serial ports for printers, modems, AppleTalk, and other serial I/O devices
- a SCSI connection for devices such as hard disk drives
- an interface to the Apple SuperDrive floppy disk drive

For video interface information, see “Built-in Interface for Video Monitors,” later in this chapter. For sound interface information, see “Sound I/O,” later in this chapter.

Apple Desktop Bus

The Apple Desktop Bus (ADB) is an asynchronous serial communication bus used to connect relatively slow user-input devices to Macintosh computers. Its software characteristics are described in *Inside Macintosh: Operating System Utilities.* One ADB connector is located on the back panel of Power Macintosh computers. It is a 4-pin mini-DIN socket, as shown in Figure 3-1.

Figure 3-1 ADB socket



The ADB pin assignments are shown in Table 3-1.

Table 3-1 ADB pin assignments

Pin	Description
1	Data; grounded by an open collector or pulled to +5 V through 470 Ω
2	Power on, fed by +5 V through 100 kΩ; connect to pin 4 to turn on the system
3	+5 V at 500 mA maximum drain; protected by a 1.25-A circuit breaker
4	Ground return

Ethernet Port

All models of Power Macintosh computers contain built-in support for Ethernet. The user can plug a drop-box cable (available from Apple or from third-party vendors) into a standard Ethernet connector on the computer.

The Ethernet port pin assignments are shown in Table 3-2.

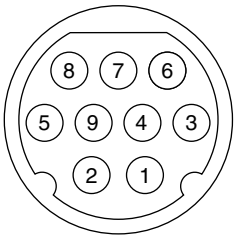
Table 3-2 Ethernet port pin assignments

Pin	Description	Pin	Description
1	+5 V	8	+5 V
2	DI+	9	DO+
3	DI–	10	DO–
4	Ground	11	Ground
5	CI+	12	No connection
6	CI–	13	No connection
7	+5 V	14	+5 V

Serial Ports

The back panel on all models of Power Macintosh computers contains two I/O ports for serial telecommunications data. Both sockets accept 9-pin plugs, as shown in Figure 3-2.

Figure 3-2 Serial port connector



Either port can be independently programmed for asynchronous or synchronous communication formats up to 9600 baud, including AppleTalk and the full range of Apple GeoPort protocols. Through these ports, the computer can communicate with a variety of ISDN and other telephone transmission facilities by using external pods.

Table 3-3 gives the pin assignments for both serial ports.

Table 3-3 Serial port pin assignments

Pin	Name	Function
1	$SCLK_{out}$	Reset pod or get pod attention
2	$Sync_{in}$ / $SCLK_{in}$	Serial clock from pod (up to 920 Kbit/sec.)
3	TxD–	Transmit –
4	Gnd / shield	Ground
5	RxD–	Receive –
6	TxD+	Transmit +
7	Wakeup / TxHS	Wake up CPU or do DMA handshake
8	RxD+	Receive +
9	+5 V	Power to pod (350 mA maximum)

SCSI Connection

The SCSI interface in Power Macintosh computers exists in two forms: an internal 50-pin ribbon connector for internal devices and an external DB-25 connector for external devices.

Power Macintosh computers contain space for the numbers of internal SCSI devices shown in Table 3-4. All models accept up to a total of seven internal and external SCSI devices combined.

Table 3-4 Spaces for internal SCSI devices

Power Macintosh model	CD-ROM drive	Hard disk drives (up to 500 MB each)	Hard disk drives (up to 1 GB each)
6100/60 and 6100/60AV	1	1	0
7100/66 and 7100/66AV	1	2	0
8100/80 and 8100/80AV	1	2	1

The standard SCSI interface transfers data at a maximum rate of 5 MB per second. It is electrically and mechanically compatible with SCSI interfaces on other computers of the Macintosh family.

In addition, the Power Macintosh 8100/80 and 8100/80AV contain a second internal SCSI cable that provides a fast SCSI interface to internal devices. This fast SCSI interface, which can transfer data at 10 MB per second, uses a ribbon cable and connector identical to the standard SCSI internal cable. Internal SCSI devices may be connected to either cable. In the shipping configurations of the Power Macintosh 8100/80 and 8100/80AV, the internal hard disk is connected to the fast SCSI cable and the internal CD-ROM drive (if any) is connected to the standard SCSI cable. Both cables are separately terminated as described in "Automatic SCSI Termination," later in this chapter.

Power Budgets

The maximum continuous power budget available for each SCSI device attached to a Power Macintosh computer is shown in Table 3-5.

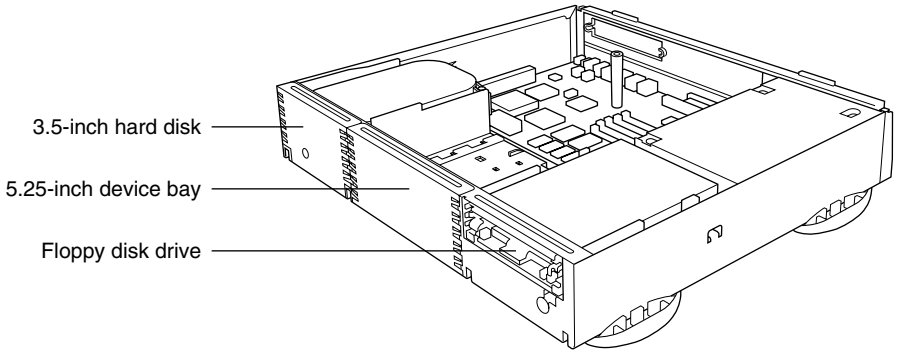
Table 3-5 SCSI power budget

Power Macintosh model	+5 V	+12 V
6100/60 and 6100/60AV	1.5 A	1.5 A
7100/66 and 7100/66AV	1.5 A	4.3 A
8100/80 and 8100/80AV	1.5 A	4.3 A

Internal SCSI Locations

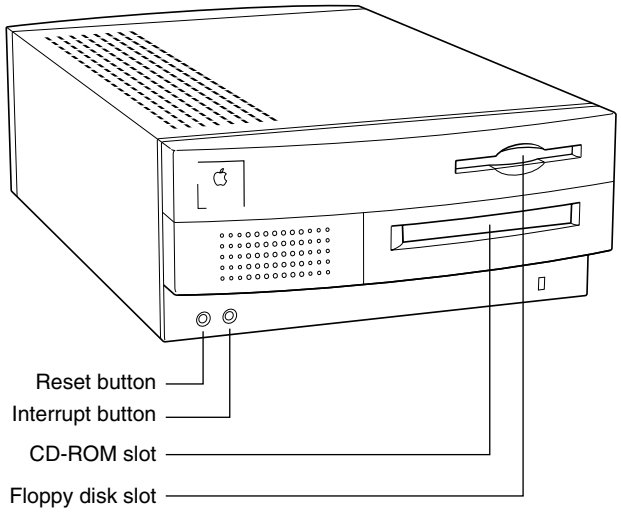
The locations of internal SCSI devices in the Power Macintosh 6100/60 and 6100/60AV are shown in Figure 3-3.

Figure 3-3 Power Macintosh 6100/60 and 6100/60AV internal SCSI device locations



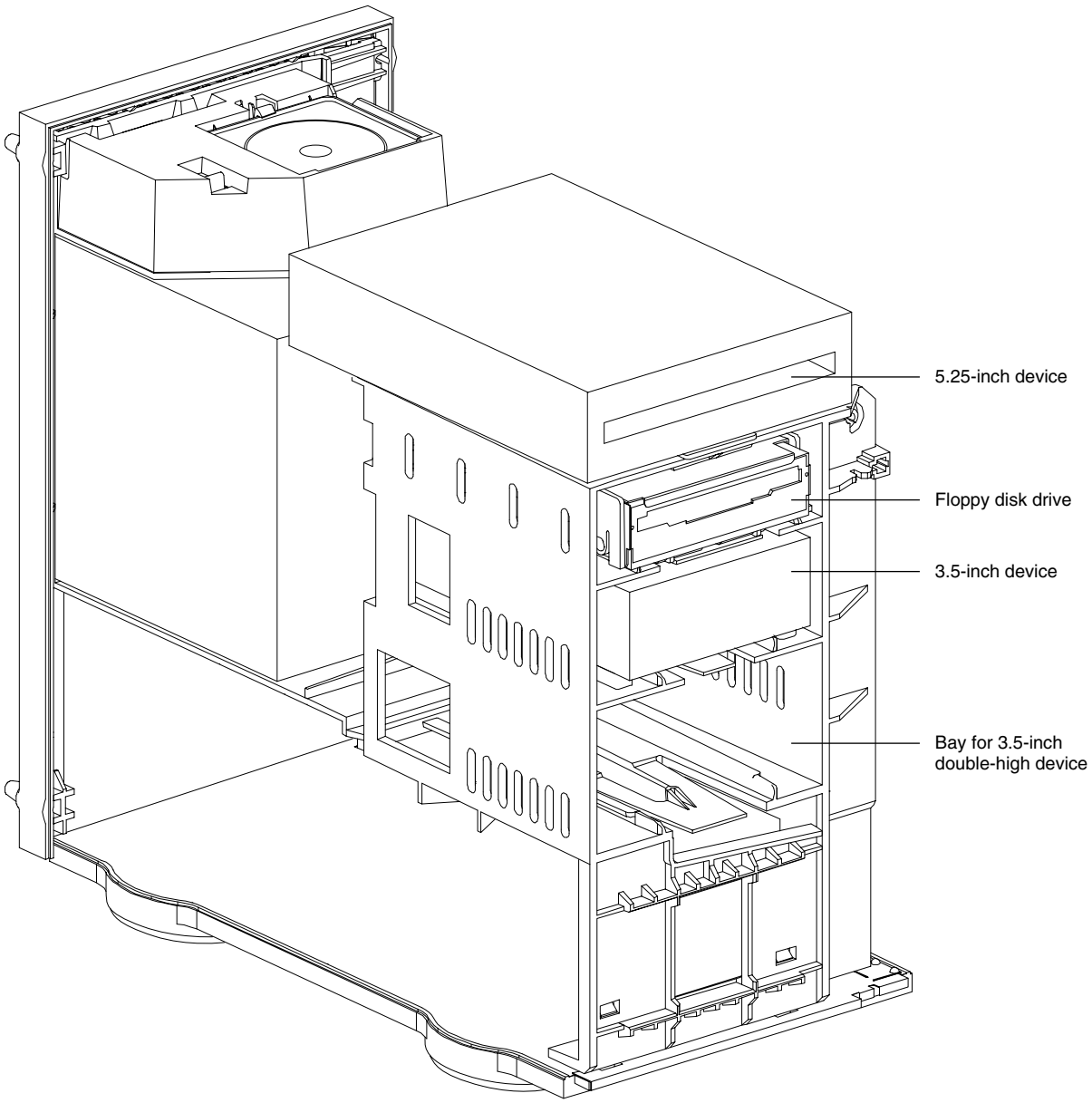
The location of the built-in CD-ROM drive in the Power Macintosh 7100/66 and 7100/66AV is shown in Figure 3-4.

Figure 3-4 Power Macintosh 7100/66 and 7100/66AV CD-ROM location



The locations of the internal SCSI devices in the Power Macintosh 8100/80 and 8100/80AV are shown in Figure 3-5.

Figure 3-5 Power Macintosh 8100/80 and 8100/80AV internal SCSI device locations



Pin Assignments

The standard internal and external SCSI pin assignments for all models of Power Macintosh computers are shown in Table 3-6.

Table 3-6 SCSI pin assignments

Pin number			Pin number		
Internal	External	**Description**	Internal	External	**Description**
1	7	Ground	2	8	/DATA0*
3	9	Ground	4	21	/DATA1
5	14	Ground	6	22	/DATA2
7	16	Ground	8	10	/DATA3
9	18	Ground	10	23	/DATA4
11	24	Ground	12	11	/DATA5
13		Ground	14	12	/DATA6
15		Ground	16	13	/DATA7
17		Ground	18	20	/DATAP
19		Ground	20		No connection
21		Ground	22		No connection
23		Ground	24		No connection
25		No connection	26	25	TERMPWR
27		Ground	28		No connection
29		Ground	30		No connection
31		Ground	32	17	/ATN
33		Ground	34		No connection
35		Ground	36	6	/BUSY
37		Ground	38	5	/ACK
39		Ground	40	4	/RST
41		Ground	42	2	/MSG
43		Ground	44	19	/SEL
45		Ground	46	15	/C/D
47		Ground	48	1	/REQ
49		Ground	50	3	/I/O

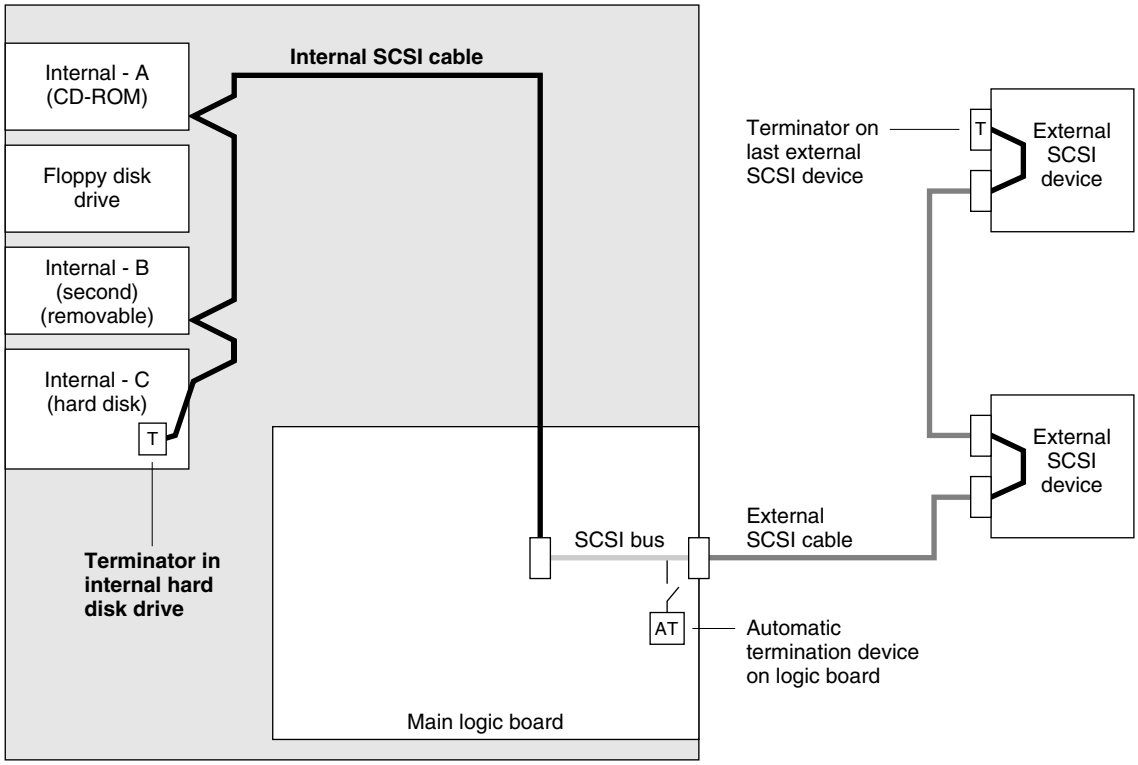
* A slash before a signal name indicates that it is in the low state when active.

Automatic SCSI Termination

Because the internal portion of the SCSI bus must be long enough to connect multiple devices, the bus requires termination at both ends. As on other Macintosh models, the external end of the bus is normally terminated at the last external device. On Power Macintosh computers, the internal end of the bus—the end at the last internal hard disk drive—is terminated in the drive itself.

Figure 3-6 shows the arrangement of the SCSI cables and terminators in a typical Power Macintosh configuration. In all Power Macintosh models, the standard SCSI bus is continuous across the internal SCSI cable, the SCSI bus traces on the logic board, and the external SCSI cable (if any). In the Power Macintosh 8100/80 and 8100/80AV, a second internal SCSI bus is driven separately by the fast SCSI controller and is separately terminated. The Power Macintosh 6100/60 can contain a maximum of two internal SCSI devices.

Figure 3-6 SCSI bus terminators



Power Macintosh computers include a feature (similar to that in Macintosh Quadra 840AV and Macintosh Centris 660AV computers) that automatically provides the proper termination when no external device is connected—that is, when the SCSI bus ends at the external connector. When no external device is connected, special circuitry terminates the bus on the logic board near the external connector. When one or more external SCSI

devices are connected, the circuitry detects the external termination during system reset and disconnects the termination on the logic board. In Figure 3-6, the box marked AT on the logic board indicates the automatic termination device.

Signals on the SCSI bus are usually connected to open-collector devices that can pull the line low but that depend on external power to pull it high. The bus includes a line called TERMPWR that provides pull-up power. The standard Macintosh terminator block used at the last external SCSI device terminates each line with a 220 Ω pull-up resistor and a 330 Ω resistor to ground.

Installing Internal SCSI Devices

In Power Macintosh computers, the device at the end of the internal SCSI cable includes a terminator; all other internal devices do not. When installing internal SCSI devices, the installer must make sure that the device at the end of the cable has a terminator and must remove terminators from any other internal SCSI devices.

SCSI termination can be present on only the last internal device—the one at the end of the internal SCSI cable. If none of the internal devices is terminated, the computer will malfunction; if more than one internal device includes terminators, the computer will malfunction and the logic board may be damaged.

As in all SCSI installations, all devices on the SCSI bus must have different ID numbers.

Floppy Disk Drive Connection

All Power Macintosh models contain one internal Apple SuperDrive floppy disk drive, which supports GCR and MFM formats for 1.44 MB disks. Unlike previous Apple floppy disk drives, the one used in Power Macintosh computers does not automatically pull in the floppy disk when the user inserts it. Table 3-7 gives the pin assignments for the 20-pin floppy disk drive connector.

Table 3-7 Floppy disk drive connector pin assignments

Pin	Signal	Description	Pin	Signal	Description
1	GND	Ground	7	GND	Ground
2	PH0	Phase 0 state control	8	PH3	Phase 3 register write strobe
3	GND	Ground	9	NC	No connection
4	PH1	Phase 1 state control	10	/WRREQ*	Write data request
5	GND	Ground	11	+5 V	+5 V
6	PH2	Phase 2 state control	12	SEL	Head select

continued

Table 3-7 Floppy disk drive connector pin assignments (continued)

Pin	Signal	Description	Pin	Signal	Description
13	+12 V	+12 V	17	+12 V	+12 V
14	/ENBL	Drive enable	18	WR	Write data
15	+12 V	+12 V	19	+12 V	+12 V
16	RD	Read data	20	NC	No connection

* A slash before a signal name indicates that it is in the low state when active.

Built-in Interface for Video Monitors

All Power Macintosh computers have support built into the main logic board for video monitors up to 16 inches in size, using system RAM for frame buffering. In addition, certain models are shipped with video expansion cards plugged into their PDS connectors. These cards provide a second channel of monitor or video support through a separate set of connectors. The video expansion cards shipped with Power Macintosh computers are the following:

- All Power Macintosh 8100/80 configurations except the Power Macintosh 8100/80AV include the Power Macintosh 8100 VRAM expansion card.
- All Power Macintosh 7100/66 configurations except the Power Macintosh 7100/66AV include the Power Macintosh 7100 VRAM expansion card.
- The Power Macintosh 8100/80AV, 7100/66AV, and 6100/60AV models include the AV card.
- Power Macintosh 6100/60 configurations other than the Power Macintosh 6100/60AV do not include any video expansion cards. They include only the monitor interface that is built into the main logic board.

For further details of the equipment shipped with these models, see “Models and Configurations,” in Chapter 1.

This section describes the video monitor interface common to all models of Power Macintosh computers; the interfaces for the video expansion and video I/O cards that are shipped with certain specific models are described in succeeding sections.

AudioVision Monitor Support

Power Macintosh computers connect to external monitors by means of an AudioVision HDI-45 monitor socket located on their back panel. In addition to the Apple AudioVision 14 monitor, this interface supports the other monitors listed in Table 3-8.

Table 3-8 Monitors supported by built-in video

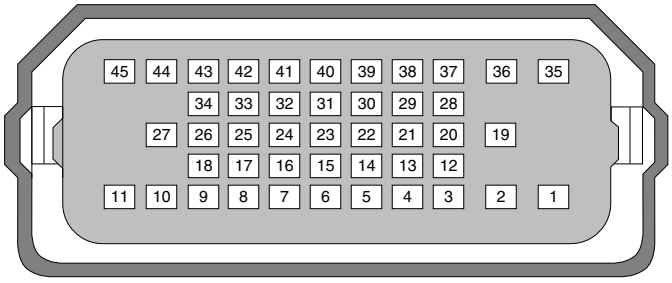
Monitor	Size (pixels)	Color depth (bits)	Frame size (bytes)
12-inch RGB	512 by 384	16	393,216
14-inch RGB	640 by 480	16	614,400
15-inch portrait	640 by 870	8	556,800
16-inch RGB	832 by 624	8	519,168
VGA	640 by 480	8	307,200

A signal timing diagram for these monitors is given in the next section.

Apple Technical Note 326 contains full information about connecting various monitors to Macintosh computers, including Power Macintosh models. This information includes details of ID codes assigned to Apple and some third-party monitors, plus hard-wire connections that let monitors assert their ID codes and therefore support automatic system configuration during startup. Apple Technical Note 144 contains additional information about color monitors. Technical Note 326 and Technical Note 144 are both described in “Supplementary Documents,” in the preface.

Figure 3-7 shows the AudioVision HDI-45 video monitor connector.

Figure 3-7 AudioVision monitor connector



Pin assignments for the AudioVision connector are given in Table 3-9.

Table 3-9 AudioVision connector pin assignments

Pin	Description	Pin	Description
1	Analog audio ground	24	Reserved
2	Audio input shield	25	Reserved
3	Left channel audio input	26	Red ground (shield)
4	Right channel audio input	27	Red video output (75 Ω)
5	Left channel audio output	28	I^2C data signal*
6	Right channel audio output	29	I^2C clock signal*
7	Reserved	30	Reserved
8	Monitor ID sense line 1†	31	Monitor ID
9	Monitor ID sense line 2†	32	Monitor ID
10	Green ground (shield)	33	Vertical sync signal
11	Green video output (75 Ω)	34	Composite sync signal
12	Video input power ground	35	ADB power +5 V
13	Power for camera +5 V	36	ADB ground
14	Reserved	37	ADB data
15	Reserved	38	Keyboard switch
16	Reserved	39	Reserved
17	Reserved	40	Reserved
18	Monitor ID sense line 3†	41	Monitor ID
19	S-video input shield	42	Horizontal sync signal
20	S-video input luminance (Y)	43	Video sync ground
21	S-video input chroma (C)	44	Blue ground (shield)
22	Reserved	45	Blue video output (75 Ω)
23	Reserved		

* Philips serial bus interface.
† See Apple Technical Note 326.

Monitor Output Timing

Figure 3-8 shows a general video timing diagram for Apple monitors.

Figure 3-8 Video timing diagram

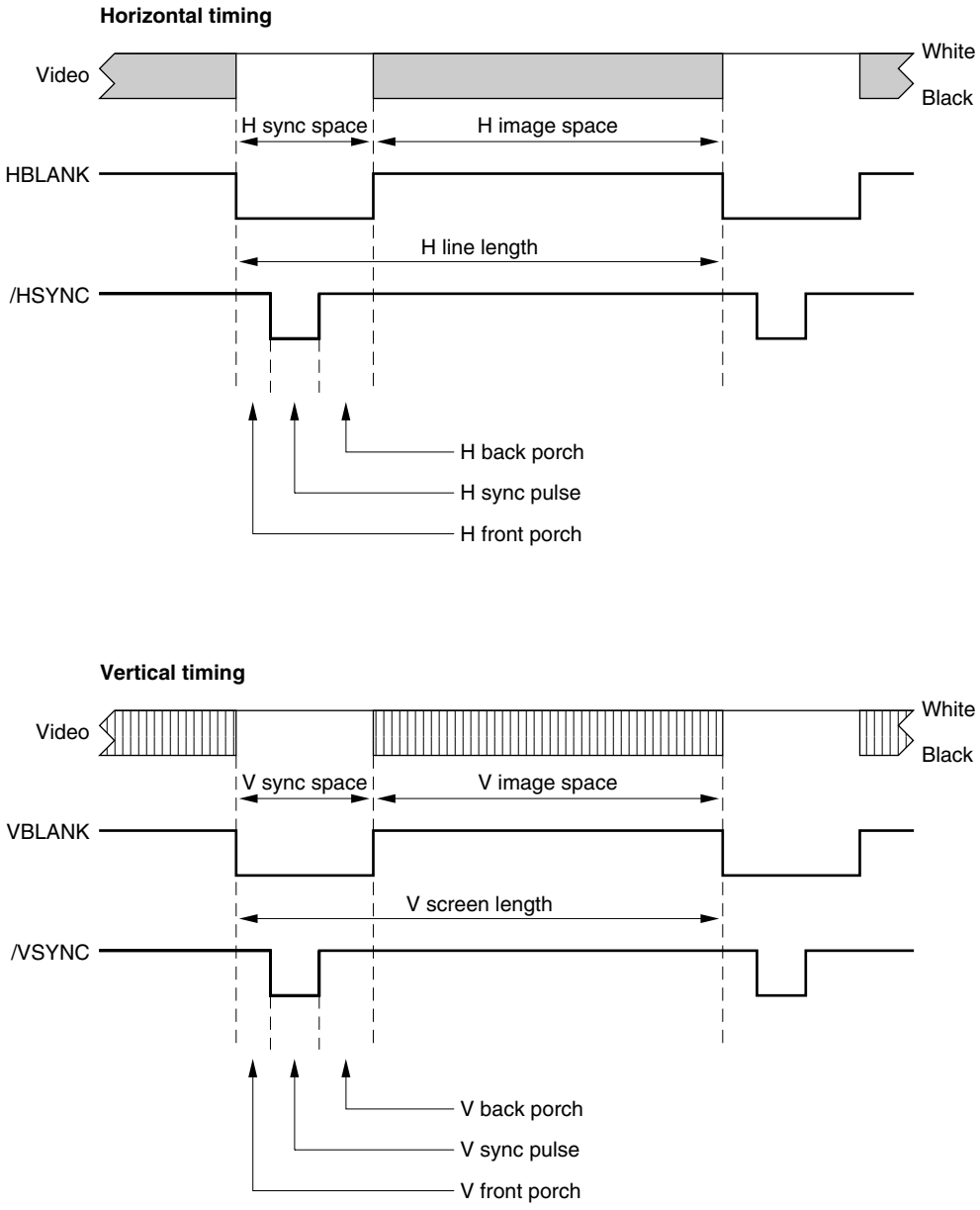


Table 3-10 gives timing values for the monitors supported by built-in circuitry. Most of the parameters listed in Table 3-10 are diagrammed in Figure 3-8.

Table 3-10 Apple monitor timing values

Parameter	12" RGB	13" RGB	Portrait	16" RGB	VGA
Image size, pixels	512 by 384	640 by 480	640 by 870	832 by 624	640 by 480
Dot clock, MHz	15.6672	31.3344	57.2832	57.2832	25.175
Dot interval, ns	63.83	31.91	17.457	17.457	39.72
Line rate, kHz	24.480	34.975	68.850	49.725	31.469
Line interval, µs	28.571	31.778	14.527	16.600	31.778
Frame rate, Hz	60.15	66.62	75.00	74.55	59.94
Frame interval, ms	16.625	15.011	13.333	13.414	16.683
H sync space, dots	128	256	192	320	160
H image space, dots	512	640	640	832	640
H line length, dots	640	896	832	1152	800
H front porch, dots	16	80	32	32	16
H sync pulse, dots	32	64	80	64	96
H back porch, dots	80	112	80	224	48
V sync space, lines	23	45	48	43	45
V image space, lines	384	480	870	624	480
V screen length, lines	407	525	918	667	525
V front porch, lines	1	3	3	1	10
V sync pulse, lines	3	3	3	3	2
V back porch, lines	19	39	42	39	33

VRAM Expansion Cards

VRAM expansion cards are Apple cards that plug into the PDS slots of Power Macintosh computers. They provide an additional DB-15 monitor output and an 80-ns VRAM frame buffer, to support larger monitors and greater color depths than are compatible with the built-in video support. There are two models of VRAM expansion cards:

- The Power Macintosh 7100 VRAM expansion card adds 1 MB of VRAM to the Power Macintosh 7100/66. The user can increase VRAM to 2 MB by adding SIMMs to the card.

- The Power Macintosh 8100 VRAM expansion card adds 2 MB of VRAM to the Power Macintosh 8100/80. The user can increase VRAM to 4 MB by adding SIMMs to the card.

Table 3-11 lists the maximum size of the monitors that can be used with each VRAM expansion card, in addition to the monitors supported by the computer's built-in circuitry (listed in Table 3-8). Each card listed in Table 3-11 can also support the monitors listed earlier in the table.

Table 3-11 Monitors supported by VRAM expansion cards

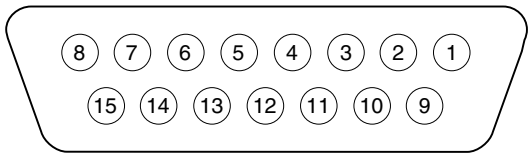
Power Macintosh model	VRAM size (MB)	Monitor size (inches)	Image size (pixels)	Maximum color depth (bits)
7100/66	1	12	512 by 384	16
	1	13–14	640 by 480	16
	1	15	640 by 870	8
7100/66 or 8100/80	2	16	832 by 624	24
	2	21	1152 by 870	16
8100/80	4	21	1152 by 870	24

The software address of the VRAM expansion cards in pseudo-slot space is $E.

Output of the VRAM expansion cards is a DB-15 connector, compatible with most Apple monitors. Apple AudioVision monitors require an adapter cable, described in "I/O Accessories," in Chapter 1. Some popular monitor types are listed in the left column of Table 3-13.

Figure 3-9 shows the physical form of the DB-15 video monitor connector.

Figure 3-9 DB-15 video monitor connector



Pin assignments for the DB-15 video monitor connector are given in Table 3-12.

Table 3-12 DB-15 video monitor pin assignments

Pin	Description	Pin	Description
1	Red ground	9	Blue video signal
2	Red video signal	10	Monitor sense 2
3	Composite synchronization	11	Synchronization ground
4	Monitor sense 0	12	Vertical synchronization
5	Green video signal	13	Blue ground
6	Green ground	14	Horizontal synchronization
7	Monitor sense 1	15	Horizontal synchronization ground
8	No connection		

AV Card

The AV card is an Apple expansion card that plugs into the PDS slot of any Power Macintosh computer. It contains a sophisticated I/O system that handles video input and output signals, mixes video with 16-bit graphics, and supports a wide variety of Apple and third-party monitors. The AV I/O system also lets the user connect a television set as a monitor, using either NTSC or PAL format.

The AV card extends the Power Macintosh computer's video capabilities to include the video capture and output features of the Apple AV Technologies. These video features were introduced with the Macintosh Centris 660AV and Macintosh Quadra 840AV computers; they are described in *Macintosh Developer Note Number 5* (listed in "Supplementary Documents," in the preface).

Power Macintosh models 6100/60AV, 7100/66AV, and 8100/80AV are shipped with the AV card installed. On the Power Macintosh 6100/60AV, the AV card uses an angle adapter card that is similar to the one shown in Figure 4-1 on page 53 but without a BART chip.

A 60-pin connector on the AV card implements the Macintosh **digital audio/video (DAV) interface.** The DAV connector taps into the AV card's unscaled YUV video input signal; through the PDS interface, it also connects to the digital audio signal input for the AWAC sound chip. NuBus cards for the Power Macintosh 7100/66AV and 8100/80AV can be designed with a flat ribbon cable that plugs into the DAV connector on the AV card, so they can access these video and audio signals directly. The DAV connection is described in "DAV Interface," in Chapter 4, and in *Macintosh DAV Interface for NuBus Expansion Cards,* bundled with this developer note in *Macintosh Developer Note Number 8.*

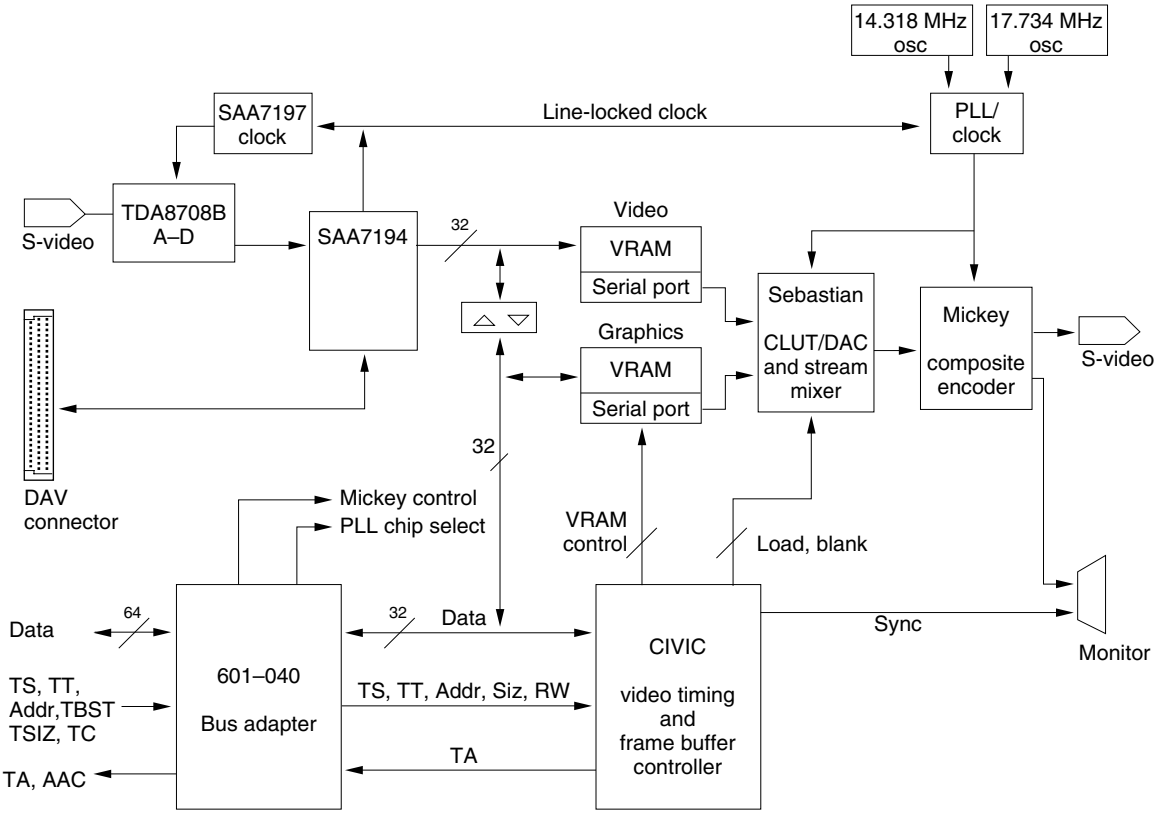
Power Macintosh models 6100/60AV, 7100/66AV, and 8100/80AV are shipped with two adapter cables so the user can connect their AV cards to standard television sets, videocams, videodisc players, and videocassette recorders. The input cable connects the signal pin of an RCA socket to pin 3 (the luminance signal) of the AV card's video input connector; the output cable connects pin 5 (the composite video signal) of the AV card's video output connector to the signal pin of an RCA plug.

Pin assignments for the AV card's video input and output connectors are given in Table 3-14 on page 45.

The software address of the AV card in pseudo-slot space is $E.

The AV card's video system is shown in Figure 3-10.

Figure 3-10 AV card block diagram



The video and graphics I/O system shown in Figure 3-10 is built around two banks of 80-ns VRAM with a total capacity of 2 MB. The CIVIC chip manages this VRAM and provides timing and interrupt signals. Applications can use the VRAM in two ways:

- as a single frame buffer that uses all the VRAM capacity
- as two frame buffers, one for video and one for graphics

If the VRAM is configured as a single video frame buffer, it can all be used for graphics and the video input can be disabled. If the VRAM is configured as two frame buffers, it can store video as well as graphics.

Video Output

Video images and graphics images stored in VRAM may have different color depths. The two images exit VRAM through its serial access memory port and pass to the Sebastian color palette chip. Sebastian provides independent color lookup tables for video and graphics images and mixes them into a single digital RGB data stream. The Sebastian then converts the result into analog RGB video, using internal DAC circuits.

Analog RGB data passes to the Mickey encoder chip. Mickey either sends RGB directly to the monitor connector or encodes it into NTSC or PAL video signals in composite or S-video format and sends it to other connectors located on the card.

The AV card has four banks of VRAM soldered in, each of which provides 0.5 MB of storage. Two of the banks can supply a graphics screen image for monitors of small size or low color depths, letting the other two banks supply live video to be mixed with the graphic image. All four banks together can support graphics alone on monitors that are larger or that use more bits per pixel.

The AV card can support mixed video and graphics in full 24-bit color on small and medium-sized monitors and in 16-bit or 8-bit color on larger monitors. The color depths (in bits per pixel) that are available when the AV card drives Apple monitors are listed in Table 3-13.

Table 3-13 Monitor color depths

Monitor type	Screen size (hor. by vert.)	Color depths	
		Graphics	Graphics/video
12-inch RGB*	512 by 384	32	32 / 16
	560 by 384	32	16 / 16
13-inch RGB	640 by 400	32	16 / 16
	640 by 480	32	16 / 16
	704 by 512	32	16 / 16
12-inch monochrome	640 by 480	8	8 / 8
Full-page monochrome	640 by 870	8	8 / 8
16-inch RGB*	832 by 624	32	16 / 16
19-inch RGB	1024 by 768	16	8 / 8†
Two-page monochrome	1152 by 870	8	8 / 8
Two-page RGB	1152 by 870	16	8 / 8
VGA*	640 by 480	32	16 / 16
Super VGA 56 Hz*	800 by 600	32	16 / 16
Super VGA 72 Hz*	800 by 600	32	16 / 16

continued

Table 3-13 Monitor color depths (continued)

Monitor type	Screen size (hor. by vert.)	Color depths	
		Graphics	Graphics/video
21-inch RGB	1152 by 870	16	8 / 8†
Super VGA 60 Hz	1024 by 768	16	8 / 8†
Super VGA 70 Hz	1024 by 768	16	8 / 8†
NTSC	640 by 480	32	16 / 16
	512 by 384	32	16 / 16
Convolved NTSC	640 by 480	8	n.a.
	512 by 384	8	n.a.
PAL	768 by 576	32	16 / 16
	640 by 480	32	16 / 16
Convolved PAL	768 by 576	8	n.a.
	640 by 480	8	n.a.

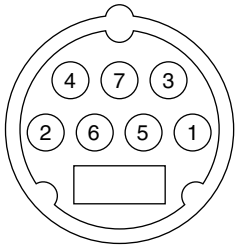
* With a color depth of 16 bits in these configurations, the maximum video window size is limited. If the video window width is 512 pixels or less, the height may be as large as 512 pixels; if the video window width is more than 512 pixels, the height is limited to 340 pixels.
† Video mode supported to 8-bit grayscale only.

The color depths in Table 3-13 are shown as the number of bits in which the color or grayscale value of each pixel can be encoded.

The AV card contains a DB-15 monitor connector. The physical form and pin assignments of this connector are given in the previous section.

The AV card also contains two identical connectors for video input and output, with adapter cables for composite video devices that have RCA connectors, such as television equipment. The mechanical configuration of the video connectors is shown in Figure 3-11. Their pin assignments are given in Table 3-14.

Figure 3-11 Video input and output connectors



Video Inputs

Video input signals, which may be analog composite or S-video in NTSC, PAL, or SECAM format, enter through the connector shown in Figure 3-11. An adapter cable included with Power Macintosh AV models receives composite video from external devices that have RCA connectors and feeds it into the luminance input of the TDA8708 video ADC chip. The ADC chip can also receive separate luminance and chroma signals from S-video sources. The ADC chip digitizes the video waveform and the SAA7194 chip decodes the result into YUV format. The YUV digital video format, also known as YCrCb, is described in CCIR *Recommended Standard 601-2*, which is listed in "Supplementary Documents," in the preface.

The SAA7194 chip scales down the video image and converts its format to either 8-bit grayscale, 15-bit RGB, or 16-bit YUV, storing the result in the VRAM buffer.

The video input and output connectors on the AV card are identical. Their pin assignments are shown in Table 3-14.

Table 3-14 Pin assignments for video I/O connectors

Pin	Input connector	Output connector
1	AGND	AGND
2	AGND	AGND
3	Video Y (luminance)	Video Y (luminance)
4	Video C (chroma)	Video C (chroma)
5	I^2C clock (Philips serial bus)	Composite video
6	+12 V at 250 mA maximum*	No connection
7	I^2C data (Philips serial bus)	No connection

* Fused at 1.1 A.

The data rate for full-screen NTSC video (640 by 480 pixels at 30 frames per second) is 18.43 MB per second through the AV card. The data rate for full-screen PAL video (768 by 576 pixels at 25 frames per second) is 22.12 MB per second. This means that it is practical to record a video image up to one-quarter screen in size on an output device such as an external hard disk drive in real time, without data compression. Larger video windows can be recorded on a Power Macintosh 8100/80AV internal hard disk, using the fast SCSI interface.

Users of the Power Macintosh 6100/60AV, 7100/66AV, or 8100/80AV can capture live color video with a standard videocam, using the composite video input cable supplied with the computer.

Sound I/O

All Power Macintosh computers contain external stereo mini phone jacks for sound I/O, connected through amplifiers to the AWAC chip. The sound system achieves simultaneous 16-bit broadcast-quality stereo sound input and output, using four 8 KB buffers, and supports Apple's speech synthesis and recognition software.

The sound I/O signals for Power Macintosh computers are described in Table 3-15.

Table 3-15 Sound connections

Panel label	Description
Audio In	8 kΩ impedance, 2 V rms maximum, 22.5 dB gain available
Audio Line Out	37 Ω impedance, 0.9 V rms maximum, attenuated –22.5 dB (crosstalk degrades from –80 dB to –32 dB when the audio output is connected to 32 Ω headphones)

Sound I/O bandwidth is 20 Hz to 20 kHz, plus or minus 2 dB. Harmonic distortion and noise total less than 0.05 percent over the bandwidth with a 1 V rms sine wave input. The input signal-to-noise ratio (SNR) is 82 dB, and the output SNR is 85 dB, with no audible discrete tones.

All Power Macintosh computers are supplied with a built-in speaker. Software can control the volume of sound to the built-in speaker and to the sound output connector independently.

The sound codec in the AWAC chip uses time-division multiplexing to transfer multiple audio channels between the PDS connector and the AMIC for DMA transfers to and from RAM memory. The signals at the PDS connector are routed to the DAV interface on the AV card, becoming available to NuBus cards in the Power Macintosh 7100/66AV and 8100/80AV. This process is described in "DAV Interface," in Chapter 4.

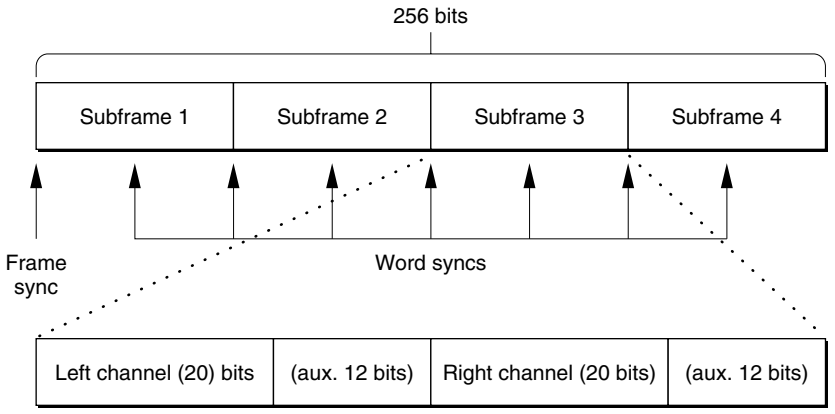
The sound signals that appear at the PDS connector are listed in Table 3-16. These signals have a minimum setup time of 10 ns and a minimum hold time of 8 ns; they can tolerate a maximum load of 20 pF.

Table 3-16 PDS connector sound signals

PDS pin	Signal	Description
70	AwacClk	Bit clock that clocks serial data on AwacDataOut and AwacDataIn; 256 times the sample rate; also used to clock AwacSync
71	AwacSync	Signal that marks the beginning of a frame and a word
72	AwacDataOut	Sound output from AMIC to PDS connector
163	AwacDataIn	Sound input from PDS connector to AMIC

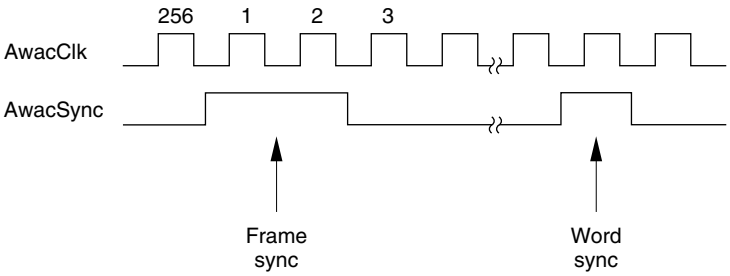
The AWAC codec transfers data in 256-bit frames, each of which contains four subframes of 64 bits each. Each subframe carries two 32-bit audio samples, one left and one right. Each sample contains 20 data bits and 12 auxiliary bits. Subframe 1 is reserved for the Macintosh system sound I/O; the other subframes are available for applications and expansion cards to use. The AWAC frame structure is shown in Figure 3-12.

Figure 3-12 AWAC sound frame



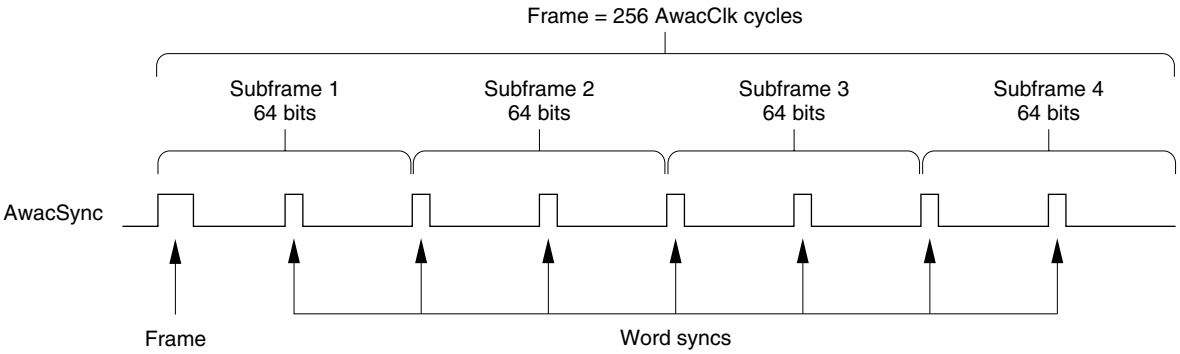
The signals AwacSync, AwacDataOut, and AwacDataIn are clocked by the AwacClk signal. The falling edge of the clock is used to clock the signals, and the rising edge is used to sample them. As shown in Figure 3-13, a frame sync is marked by a pulse two AwacClk cycles wide; a word sync is marked by a pulse one AwacSync cycle wide.

Figure 3-13 Sound frame and word synchronization



The AwacSync synchronization signals for each subframe are shown in Figure 3-14.

Figure 3-14 Sound subframe synchronization



CHAPTER 4

Expansion Capabilities

Users can expand the capabilities of Power Macintosh computers in several ways by adding plug-in cards. This chapter describes the following expansion possibilities:

- expansion cards in NuBus slots
- expansion cards in PDS slots (for the Power Macintosh 6100/60 only)
- RAM expansion SIMMs on the main logic board
- second-level cache memory expansion SIMMs on the main logic board
- VRAM expansion SIMMs on HPV cards

Each Power Macintosh model has different capabilities for accepting expansion cards, as shown in Table 4-1.

Table 4-1 Maximum expansion card capacity

	Power Macintosh model					
Card type	6100/60	7100/66	8100/80	6100/60AV	7100/66AV	8100/80AV
NuBus	1*	3	3	None	3	3
PDS	1	None	None	None	None	None
RAM	2	4	8	2	4	8
Cache	1	1	n. a.†	1	1	n. a.†
VRAM	None	4‡	4‡	None	None	None

* The Power Macintosh 6100/60 uses an optional NuBus adapter card in the PDS connector.
† Cache expansion is already installed on the Power Macintosh 8100/80 and 8100/80AV.
‡ The Power Macintosh 7100/66 and 8100/80 use different capacity VRAM SIMMs.

NuBus Interface

The NuBus interface in Power Macintosh computers provides access between RAM or ROM and plug-in expansion cards. It is not designed to let plug-in cards gain access to peripheral devices directly. However, NuBus cards for the Power Macintosh 7100/66AV and 8100/80AV can tap into the raw audio and video signals of the Apple AV Technologies, as described in "DAV Interface," later in this chapter.

The Power Macintosh 7100/66, 7100/66AV, 8100/80, and 8100/80AV models accept up to three NuBus cards. The Power Macintosh 6100/60 accepts one NuBus card by means of an optional adapter card in the PDS slot, as described in "NuBus Cards for the Power Macintosh 6100/60," later in this chapter. The Power Macintosh 6100/60AV cannot accept a NuBus card because its PDS slot is already occupied by the AV card.

The NuBus implementation in Power Macintosh computers is based on the NuBus '90 specification (ANSI/IEEE Std 1196-1990). For full technical details about NuBus, including NuBus '90, see *Designing Cards and Drivers for the Macintosh Family,* third edition. This book is listed in "Supplementary Documents," in the preface.

NuBus Slot Connections

NuBus slots in the Power Macintosh 7100/66, 7100/66AV, 8100/80, and 8100/80AV accept both long (4 by 13 inches) and short (4 by 7 inches) expansion cards of the same physical configuration as those used with Macintosh Quadra computers. The Power Macintosh 6100/60 accepts only short expansion cards, which may be the same as short cards for the Power Macintosh 8100/80 or 7100/66. For mechanical details of long and short expansion cards, see *Designing Cards and Drivers for the Macintosh Family*, third edition.

The pin assignments for the 96-pin Euro-DIN NuBus expansion card connectors in Power Macintosh computers are shown in Table 4-2.

Table 4-2 NuBus pin assignments

Pin	Name	Pin	Name	Pin	Name
A1	–12 V	B1	–12 V	C1	/RESET*
A2	SB0	B2	GND	C2	GND
A3	/SPV	B3	GND	C3	+5 V
A4	/SP	B4	+5 V	C4	+5 V
A5	/TM1	B5	+5 V	C5	/TM0
A6	/AD1	B6	+5 V	C6	/AD0
A7	/AD3	B7	+5 V	C7	/AD2
A8	/AD5	B8	/TM02	C8	/AD4
A9	/AD7	B9	/CM0	C9	/AD6
A10	/AD9	B10	/CM1	C10	/AD8
A11	/AD11	B11	/CM2	C11	/AD10
A12	/AD13	B12	GND	C12	/AD12
A13	/AD15	B13	GND	C13	/AD14
A14	/AD17	B14	GND	C14	/AD16
A15	/AD19	B15	GND	C15	/AD18
A16	/AD21	B16	GND	C16	/AD20
A17	/AD23	B17	GND	C17	/AD22
A18	/AD25	B18	GND	C18	/AD24
A19	/AD27	B19	GND	C19	/AD26
A20	/AD29	B20	GND	C20	/AD28
A21	/AD31	B21	GND	C21	/AD30
A22	GND	B22	GND	C22	GND

continued

Table 4-2 NuBus pin assignments (continued)

Pin	Name	Pin	Name	Pin	Name
A23	GND	B23	GND	C23	/PFW
A24	/ARB1	B24	/CLK2X	C24	/ARB0
A25	/ARB3	B25	STDBYPWR†	C25	/ARB2
A26	/GA1	B26	/CLK2XEN	C26	/GA0
A27	/GA3	B27	/CBUSY	C27	/GA2
A28	/ACK	B28	+5 V	C28	/START
A29	+5 V	B29	+5 V	C29	+5 V
A30	/RQST	B30	GND	C30	+5 V
A31	/NMRQx	B31	GND	C31	GND
A32	+12 V	B32	+12 V	C32	/CLK

* A slash before a signal name indicates that it is in the low state when active.
† Trickle +5 V supply.

The power available and maximum capacitance loading for each NuBus expansion card in a Power Macintosh computer are shown in Table 4-3.

Table 4-3 Power budget for each NuBus card

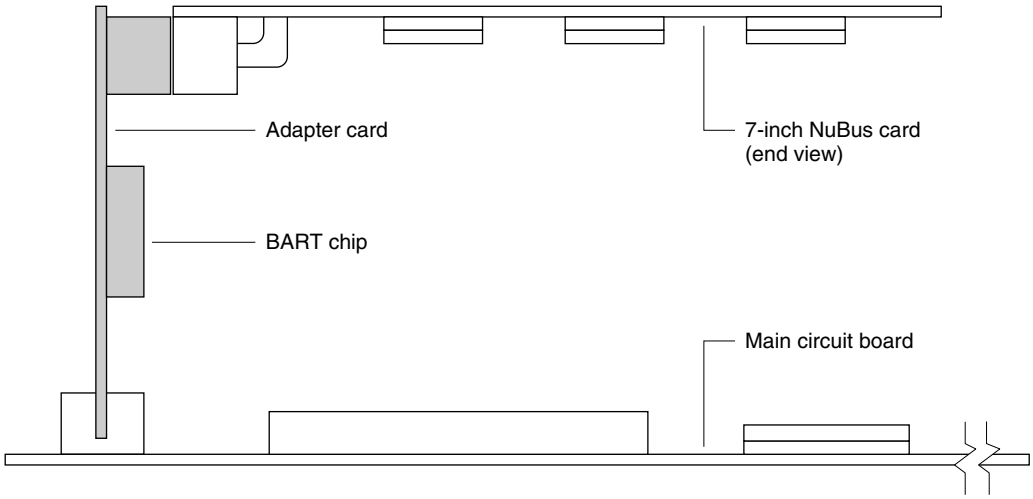
Voltage (V)	Maximum current (A)	Maximum capacitance (µF)
+5	2.0	1513
+12	0.175	536
–12	0.15	698

▲ **WARNING**
PowerPC processor–based Macintosh systems do not support locking cycles on NuBus. Resource locking will fail without a bus error being generated. For information about NuBus locking, see *Designing Cards and Drivers for the Macintosh Family,* third edition, Chapter 4. This book is listed in "Supplementary Documents," in the preface. ▲

NuBus Cards for the Power Macintosh 6100/60

Users of the Power Macintosh 6100/60 acquire NuBus expansion capability by installing an adapter card, sold separately, in the computer's PDS slot. This adapter card accepts a short NuBus expansion card, which lies parallel to the main circuit board, as shown in Figure 4-1. The adapter card carries the BART NuBus controller chip, so this chip is present in the Power Macintosh 6100/60 system only when the adapter card is installed.

Figure 4-1 Power Macintosh 6100 NuBus adapter card mounting



DAV Interface

The DAV interface is supported by a connector on the AV card that lets NuBus cards in Power Macintosh models 7100/66AV and 8100/80AV gain access to the audio and video signal streams of the Apple AV technologies. One use for the DAV interface is to provide a hardware audio or video compression capability on an accessory card, which can write out compressed data to NuBus. The DAV interface is described in detail in *Macintosh DAV Interface for NuBus Expansion Cards*, bundled with this developer note in *Macintosh Developer Note Number 8*.

Although it contains an AV card, the Power Macintosh 6100/60AV cannot exploit the DAV interface because there are no other card slots available.

The DAV connector provides access to the AV card's 4:2:2 unscaled YUV video input signal and the Power Macintosh system's digital audio signal input for the AWAC sound codec. The DAV video signal is present in the circuitry on the AV card; the DAV audio signal is passed from the main circuit board to the AV card through the PDS connector, described in the next section. The AV card and its signals are described in "AV Card," in Chapter 3. The Power Macintosh system's audio signals are described in "Sound I/O," in the same chapter.

To use the DAV interface, a NuBus card must be designed with a flat ribbon cable terminating in a plug that fits the DAV connector on the AV card. The DAV connector is a 60-pin type, model AMP 104549-8. Card designers should analyze the physical relations between the AV card location and possible NuBus card locations in the Power Macintosh 7100/66AV and 8100/80AV to determine the appropriate length and configuration of the card-to-card ribbon cable. A typical cable length is 2.5 inches.

The DAV connector pin assignments are shown in Table 4-4.

Table 4-4 DAV connector pin assignments

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	Ground	16	Ground	31	UV bit 1	46	Ground
2	Ground	17	Y bit 0	32	Ground	47	CREFB*
3	Y bit 7	18	Ground	33	UV bit 0	48	Ground
4	Ground	19	UV bit 7	34	Ground	49	DIR†
5	Y bit 6	20	Ground	35	AwacSync	50	Ground
6	Ground	21	UV bit 6	36	Ground	51	I^2C Data
7	Y bit 5	22	Ground	37	AwacSerOut	52	Ground
8	Ground	23	UV bit 5	38	Ground	53	I^2C Clock
9	Y bit 4	24	Ground	39	AwacSerIn	54	Ground
10	Ground	25	UV bit 4	40	Ground	55	Ground
11	Y bit 3	26	Ground	41	AwacBitClk	56	Ground
12	Ground	27	UV bit 3	42	Ground	57	Line-lock clock
13	Y bit 2	28	Ground	43	Vertical sync	58	Ground
14	Ground	29	UV bit 2	44	Ground	59	Ground
15	Y bit 1	30	Ground	45	HRef	60	Ground

* Clock reference qualifier.
† Expansion bus input, pulled down by 1 kΩ.

PDS Expansion Cards for the Power Macintosh 6100/60

Every Power Macintosh computer except the Power Macintosh 6100/60 is shipped with a PDS expansion card installed. For this reason, Apple does not recommend that third-party vendors offer PDS cards for these computers. The cards shipped with different models are listed in Table 1-1 on page 4 and are described in “Apple Expansion Cards,” in Chapter 1.

The Power Macintosh 6100/60 is shipped with its PDS slot empty and hence may accept a third-party PDS expansion card. However, the user of a Power Macintosh 6100/60 may choose to install a NuBus adapter card in the PDS slot instead, to give the computer a NuBus capability. In the past, most Macintosh users have preferred NuBus cards to PDS cards. The NuBus capability option is discussed in “NuBus Cards for the Power Macintosh 6100/60,” earlier in this chapter.

PDS expansion cards gain access to the PowerPC 601 processor by way of the CPU bus, described in “CPU Bus,” in Chapter 2. The pin assignments for the PDS connector in the Power Macintosh 6100/60 are given in Table 4-5.

Table 4-5 PDS connector pin assignments

Pin	Signal	Pin	Signal	Pin	Signal
1	+5 V	30	D46	59	+5 V
2	GND	31	D47	60	D48
3	–12 V	32	+5 V	61	D49
4	CPUint	33	/XferAck	62	D50
5	/KeyboardSW*	34	/XferErrAck	63	D51
6	GND	35	A1	64	GND
7	D32	36	A3	65	D52
8	D33	37	A5	66	D53
9	D34	38	A7	67	D54
10	D35	39	GND	68	D55
11	GND	40	A9	69	GND
12	D36	41	A11	70	AwacClk
13	D37	42	A13	71	AwacSync
14	D38	43	A15	72	AwacDataIn
15	D39	44	A17	73	STDBYPWR†
16	+5 V	45	+5 V	74	/PFW
17	/DBB	46	A19	75	+5 V
18	/AddrRtry	47	A21	76	D56
19	/DataRtry	48	A23	77	D57
20	/NuDump	49	A25	78	D58
21	/XferStart	50	GND	79	D59
22	GND	51	A27	80	GND
23	D40	52	A29	81	D60
24	D41	53	A31	82	D61
25	D42	54	/CacheIn	83	D62
26	D43	55	/Burst	84	D63
27	GND	56	/Rsrv	85	GND
28	D44	57	/Shared	86	+5 V
29	D45	58	/Global	87	/Reset

continued

Table 4-5 PDS connector pin assignments (continued)

Pin	Signal	Pin	Signal	Pin	Signal
88	GND	120	D13	152	D17
89	PDS CLK	121	D14	153	D18
90	GND	122	D15	154	D19
91	+5 V	123	+5 V	155	GND
92	+5 V	124	/AddrAck	156	D20
93	GND	125	/ABB	157	D21
94	+12 V	126	A0	158	D22
95	+12 V	127	A2	159	D23
96	ADB	128	A4	160	GND
97	GND	129	A6	161	TCode0
98	D0	130	GND	162	TCode1
99	D1	131	A8	163	AwacDataOut
100	D2	132	A10	164	I^2C clock
101	D3	133	A12	165	I^2C data
102	GND	134	A14	166	+5 V
103	D4	135	A16	167	D24
104	D5	136	+5 V	168	D25
105	D6	137	A18	169	D26
106	D7	138	A20	170	D27
107	+5 V	139	A22	171	GND
108	TSize0	140	A24	172	D28
109	TSize1	141	GND	173	D29
110	TSize2	142	A26	174	D30
111	NC	143	A28	175	D31
112	NC	144	A30	176	GND
113	GND	145	TType0	177	+5 V
114	D8	146	TType1	178	/PDS REQ
115	D9	147	TType2	179	/PdsGrant
116	D10	148	TType3	180	PDS IRQ2
117	D11	149	TType4	181	GND
118	GND	150	+5 V	182	+5 V
119	D12	151	D16		

* A slash before a signal name indicates that it is in the low state when active.
† Trickle +5 V supply.

RAM Expansion SIMMs

The user of a Power Macintosh computer can expand RAM capacity by inserting 72-pin SIMMs in RAM expansion slots.

IMPORTANT

RAM SIMMs must be installed in pairs. ▲

DRAM chips for Power Macintosh computers must have an access time of not more than 80 ns. RAM SIMMs must accept the column address strobe (CAS) before the row address strobe (RAS) for refresh and may have no more than eight chips per bank.

Note

All Power Macintosh models ignore the parity connection on RAM SIMMs. ◆

Possible RAM expansion configurations are shown in Table 4-6.

Table 4-6 RAM configurations

Bank size (MB)	Organization	Row address bits	Column address bits
1	256 Kbit by 4	9	9
1	1 Mbit by 4	10	10
2	512 Kbit by 8	10	9
4	4 Mbit by 4	11	11
8	2 Mbit by 8	11	10
4	4 Mbit by 4	12	10
8	2 Mbit by 8	12	9
16	1 Mbit by 16	11	9

Table 4-9 shows the RAM SIMM pin assignments.

Table 4-7 RAM SIMM pin assignments

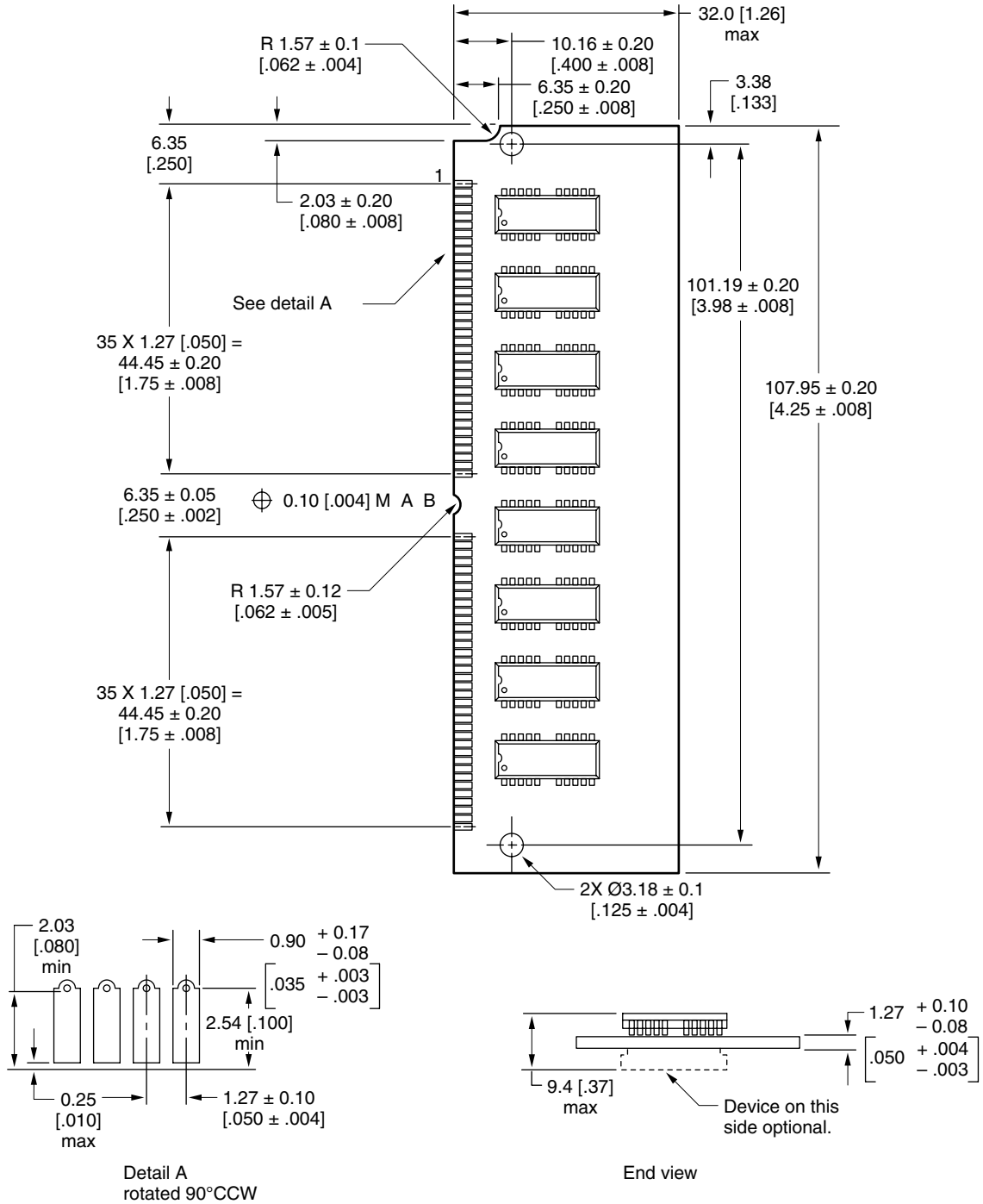
Pin	Name	Pin	Name	Pin	Name
1	GND	25	D22	49	D8
2	D0	26	D7	50	D24
3	D16	27	D23	51	D9
4	D1	28	A7	52	D25
5	D17	29	A11	53	D10
6	D2	30	+5 V	54	D26
7	D18	31	A8	55	D11
8	D3	32	A9	56	D27
9	D19	33	/RAS3*	57	D12
10	+5 V	34	/RAS2	58	D28
11	NC	35	Reserved	59	+5 V
12	A0	36	Reserved	60	D29
13	A1	37	Reserved	61	D13
14	A2	38	Reserved	62	D30
15	A3	39	GND	63	D14
16	A4	40	/CAS0	64	D31
17	A5	41	/CAS2	65	D15
18	A6	42	/CAS3	66	NC
19	A10	43	/CAS1	67	Reserved
20	D4	44	/RAS0	68	Reserved
21	D20	45	/RAS1	69	Reserved
22	D5	46	NC	70	Reserved
23	D21	47	WE	71	Reserved
24	D6	48	NC	72	GND

* A slash before a signal name indicates that it is in the low state when active.

Figure 4-2 shows the mechanical dimensions of SIMM modules for expanding RAM. Dimensions are given in millimeters, with inch equivalents in brackets.

Because of signal loading limits, there may be no more than eight chips per bank of RAM; composite SIMMs cannot be used.

Figure 4-2 RAM SIMM mechanical dimensions



Cache Expansion SIMMs

Users of the Power Macintosh 6100/60, 6100/60AV, 7100/66, or 7100/66AV can expand external cache capacity by inserting a 160-pin SIMM in a cache expansion slot. The Power Macintosh 8100/80 and 8100/80AV are shipped with cache expansion installed.

Table 4-9 shows the external cache SIMM pin assignments. Although cache parity signals are shown, they are not used in Power Macintosh systems.

Table 4-8 Cache SIMM pin assignments

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	+5 V	23	D44	45	A17	67	D57
2	GND	24	D45	46	A19	68	D58
3	+12 V	25	D46	47	A21	69	D59
4	D32	26	D47	48	A23	70	CaParity0
5	D33	27	GND	49	A25	71	+5 V
6	D34	28	/OTPRVpp	50	A27	72	/CaWE0
7	D35	29	A3	51	A29	73	D50
8	CaParity3	30	A5	52	A31	74	D51
9	+5 V	31	A7	53	GND	75	D52
10	/CaWE3*	32	A9	54	D48	76	D53
11	D36	33	A11	55	D49	77	GND
12	D37	34	A13	56	D50	78	/CaOE
13	D38	35	NC	57	D51	79	/CaAdAdv
14	D39	36	/Reset	58	CaParity1	80	+5 V
15	GND	37	/FWEH	59	+5 V	81	+5 V
16	D40	38	/ROMOEH	60	/CaWE1	82	GND
17	D41	39	/TagWR	61	D52	83	+12 V
18	D42	40	CaMatch	62	D53	84	D0
19	D43	41	+5 V	63	D54	85	D1
20	CaParity2	42	SClk 2	64	D55	86	D2
21	+5 V	43	GND	65	GND	87	D3
22	/CaWE2	44	A15	66	D56	88	/CaWE7

continued

Table 4-8 Cache SIMM pin assignments (continued)

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
89	+5 V	107	GND	125	A16	143	D22
90	CaParity7	108	ROMA3	126	A18	144	D23
91	D4	109	ROMA4	127	A20	145	GND
92	D5	110	A4	128	A22	146	D24
93	D6	111	A6	129	A24	147	D25
94	D7	112	A8	130	A26	148	D26
95	GND	113	A10	131	A28	149	D27
96	D8	114	A12	132	A30	150	/CaWE4
97	D9	115	NC	133	GND	151	+5 V
98	D10	116	/ROMEN	134	D16	152	CaParity4
99	D11	117	/FWEL	135	D17	153	D28
100	/CaWE6	118	/ROMOEL	136	D18	154	D29
101	+5 V	119	/TagSel	137	D19	155	D30
102	CaParity6	120	/TagCS	138	CaWE5	156	D31
103	D12	121	+5 V	139	+5 V	157	GND
104	D13	122	SClk1	140	CaParity5	158	/CaXFRS
105	D14	123	GND	141	D20	159	/CaCS
106	D15	124	A14	142	D21	160	+5 V

* A slash before a signal name indicates that it is in the low state when active.

VRAM Expansion SIMMs

The user of a Power Macintosh 7100/66 or 8100/80 can increase the VRAM capacity of the computer's VRAM expansion card by inserting 68-pin SIMMs in connectors on the card.

SIMMs for both VRAM expansion cards have the same pin assignments and external dimensions. However, SIMMs for the card in the Power Macintosh 7100/66 are loaded with two chips, each storing 128 Kbit by 8 bits; SIMMs for the card in the Power Macintosh 8100/80 are loaded with four chips, each storing 256 Kbit by 4 bits.

Both types of SIMMs use 80-ns VRAM chips in surface-mount packages on a four-layer circuit board.

Table 4-9 shows the VRAM SIMM pin assignments.

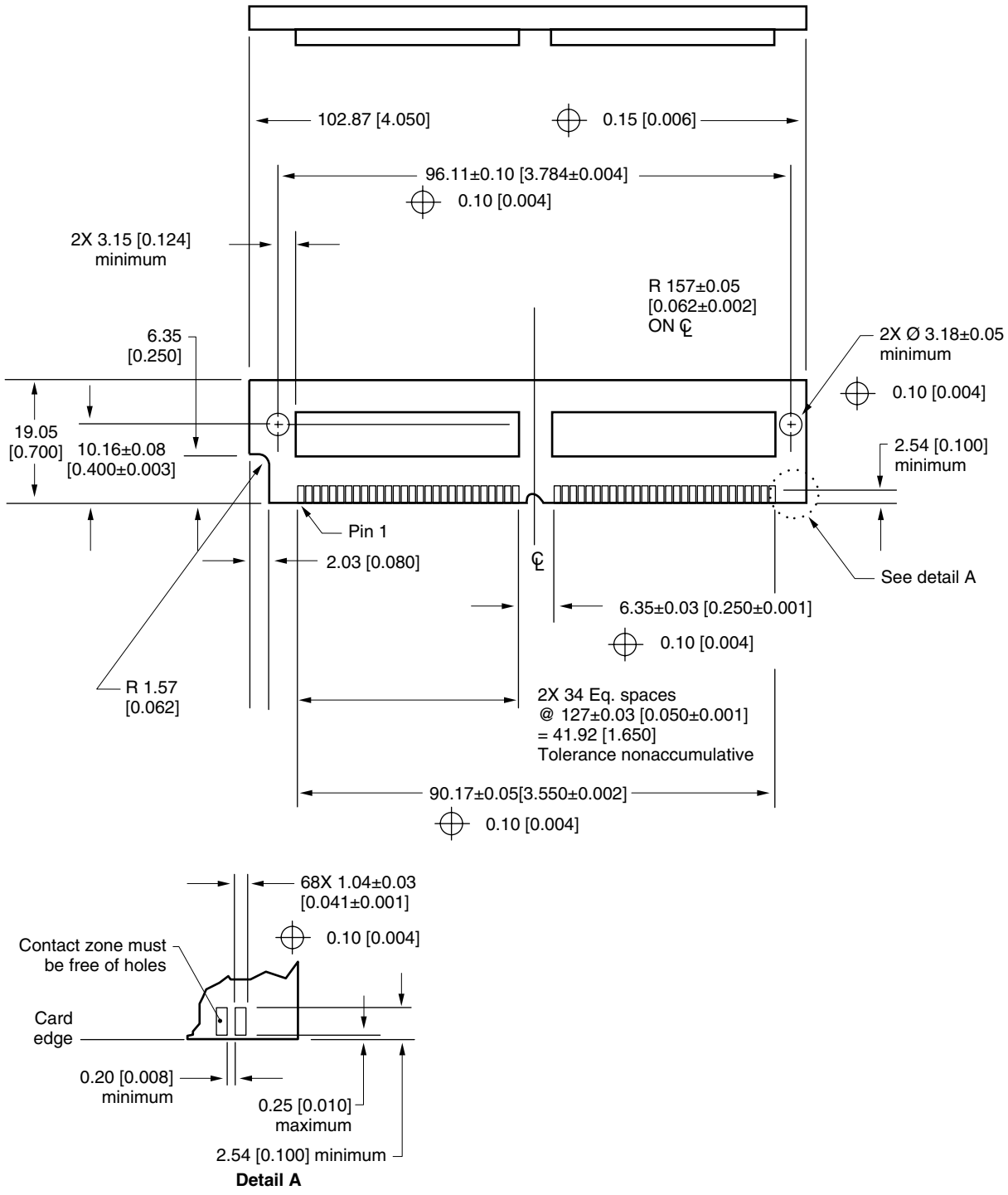
Table 4-9 VRAM SIMM pin assignments

Pin	Name	Pin	Name	Pin	Name
1	+5 V	24	DQ4	47	DQ10
2	DSF*	25	DQ5	48	A6
3	SDQ0	26	SDQ7	49	A7
4	SDQ1	27	SDQ6	50	A8
5	/DT-OE0†	28	NC	51	NC
6	DQ0	29	+5 V	52	+5 V
7	DQ1	30	DQ7	53	GND
8	SDQ3	31	DQ6	54	GND
9	SDQ1	32	/CAS0	55	SDQ12
10	/WE0	33	A4	56	SDQ13
11	/RAS	34	A5	57	NC
12	/SE0	35	GND	58	DQ12
13	DQ3	36	SC	59	DQ13
14	DQ2	37	SCQ8	60	SDQ15
15	A0	38	SDQ9	61	SDQ14
16	A1	39	/DT-OE1	62	NC
17	A2	40	DQ8	63	NC
18	A3	41	DQ9	64	DQ15
19	GND	42	SDQ11	65	DQ14
20	GND	43	SDQ10	66	/CAS1
21	SDQ4	44	/WE1	67	+5 V
22	SDQ5	45	/SE1	68	+5 V
23	NC	46	DQ11		

* The DSF pin must be tied to either +5 V or ground.
† A slash before a signal name indicates that it is in the low state when active.

Figure 4-3 shows the external mechanical dimensions of SIMM modules for expanding VRAM. Dimensions are given in millimeters, with inch equivalents in brackets. The chip configuration of SIMMs for the card in the Power Macintosh 7100/66 is shown; SIMMs for the card in the Power Macintosh 8100/80 are similar, but carry four chips instead of two.

Figure 4-3 VRAM SIMM mechanical dimensions



Appendixes

This part of the *Power Macintosh Computers Developer Note* contains two appendixes. They contain information that supplements the information in the previous chapters.

- Appendix A, “Overview of PowerPC Technology,” gives some of the background of the PowerPC RISC microprocessor and tells how it differs from CISC processors such as the Motorola MC68040 and the Intel processors.
- Appendix B, “Power Macintosh Application Development,” summarizes the process of developing application software to run on Power Macintosh computers.

Overview of PowerPC Technology

PowerPC is the name of a family of RISC microprocessors, of which the first model is the PowerPC 601. The PowerPC technology was developed jointly by Apple, IBM, and Motorola at the Somerset Design Center in Austin, Texas. PowerPC microprocessors are currently manufactured by IBM and Motorola.

Apple is committed to using PowerPC microprocessors in its future CPUs, including portable computers, desktop computers, servers, and workstations. Many other vendors of computer products are committed to this industry-standard microprocessor family.

This appendix gives a brief overview of PowerPC microprocessor technology and outlines its current and future role in Macintosh computers.

The Advantages of RISC

RISC is the acronym for **reduced instruction set computing.** It might equally well stand for *regularized* instruction set computing, for the reduced instruction set has these two important characteristics:

- All instructions have the same length and format.
- All instructions (except branches) are executed through the same procedural steps.

When an instruction set has these characteristics, it becomes possible for the processor to **pipeline** instructions with maximum efficiency—to pour them into multiple processing paths through which they are handled simultaneously. Program speed increases dramatically because the RISC processor can easily execute several instructions during each clock cycle.

The alternative to RISC is **CISC (complex instruction set computing).** Its instructions vary in length and format and may require different sequences of steps to process. As a consequence, the CISC processor must identify each instruction's type before it can read the instruction's operands and move onward. For example, it must determine whether an instruction's format is 2 bytes long or 4 bytes long before it can process the succeeding bytes in the instruction stream or find the beginning of the next instruction. The CISC processor must also handle certain kinds of instructions (such as memory moves with complex addressing) in special ways, making it difficult to pour instructions into standardized execution engines. Even using the parallel processing technique known as *superscalar processing*, any CISC processor spends much of its time either parsing the incoming instruction stream or holding up new instructions until it completes an instruction already in progress.

Today, RISC processing is needed to achieve the level of processor performance required by applications such as video handling, data compression and decompression, sophisticated sound, speech recognition and synthesis, and advanced graphics. It represents the next generation of fundamental processor technology. The transition from CISC to RISC can be interpreted in several ways:

- *As rethinking hardware to take advantage of modern programming tools.* CISC technology was originally designed to facilitate assembly-language programming and instruction-level debugging. CISC code is easier for people to read, although it is more cumbersome for a machine to process. Because programmers often worked directly with processor code, CISC technology sacrificed performance to achieve clarity of purpose and help programmers understand program flow at the execution level. With modern programming tools, however, most programming is done in higher-level languages and most debugging is done at the source level. RISC technology achieves better performance at the cost of generating code that is hard for programmers to analyze, but this is not a problem because modern compilers and debuggers generally shield programmers from having to deal directly with RISC code.
- *As making a tradeoff between performance and code length.* Memory was limited and expensive in early microcomputers, so CISC technology was designed to minimize code length. Simple instructions were made shorter than complicated instructions, and functions such as complex addressing modes were combined with processing actions to minimize the number of instructions needed to perform common tasks. Today memory cost is less of a factor, while performance is increasingly important. RISC technology achieves better performance by making all instructions the same length and by separating addressing functions from processing actions. The cost is a modest increase in code length—a burden easily absorbed in today's computing environments.
- *As a response to advances in microprocessor fabrication technology.* The cost of manufacturing a microprocessor is directly related to the number of active devices on it. Early CISC designs reduced the microprocessor's manufacturing cost by using as much external circuitry as practical. For example, they tended to use external memory chips instead of registers on the microprocessor itself. With the evolution of large-scale fabrication technology, it has become possible to include more devices on the chip at lower cost. Modern RISC processors take advantage of this evolution by adopting techniques that keep processing actions on the chip—for example, by using many local registers. The result is an increase in performance, because pieces of data are moved on and off the microprocessor chip less frequently.

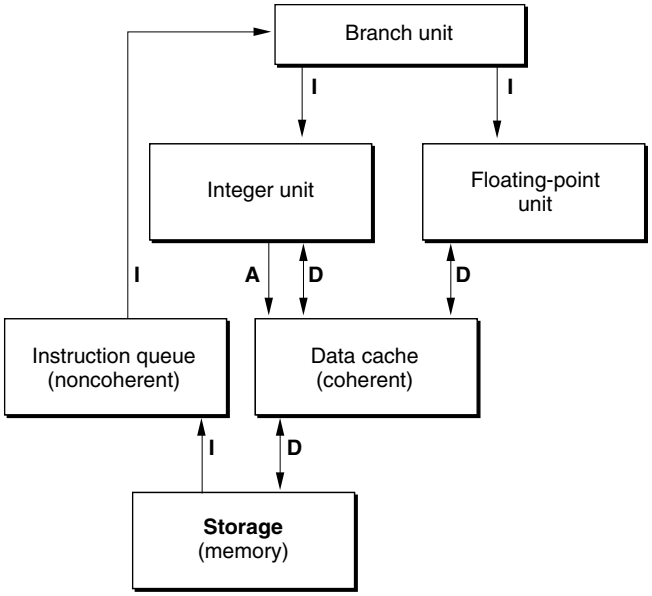
A common theme runs through the reasons just listed for the transition from CISC to RISC technology. CISC forces software to respond to hardware constraints; it makes software compensate for the cost of memory, the difficulty of fabricating large chips, and the need to work with code at the instruction level. RISC lets software achieve its maximum potential. It is a hardware design that recognizes modern software capabilities, such as the ability to break processing tasks down into simpler actions and the availability of tools that shield the programmer from having to deal with hardware issues. Because it is software-oriented, RISC supports an essential goal of many current applications—maximum execution speed.

Hence, RISC represents a better hardware environment than CISC for today's software technology. As computing becomes increasingly a software challenge and less a hardware challenge, RISC is the more appropriate technology.

PowerPC Architecture

A simplified diagram of the internal architecture of the PowerPC 601 microprocessor is shown in Figure A-1.

Figure A-1 PowerPC 601 architecture



The memory storage shown at the bottom of Figure A-1—normally, the computer's DRAM—contains the program instructions to be executed and the data to be fetched, processed, and returned. The parts of the PowerPC microprocessor that execute the instructions and process the data are discussed in the next sections.

Instruction Queue

The **instruction queue** is a first-in, first-out buffer that accepts a stream of instruction codes from memory. These codes, which constitute the program being executed, ultimately exit the instruction queue and go to the processing units. During this process, incoming instructions are also fed to the branch unit, which detects any branch instructions among them.

Branch Unit

The **branch unit** contains eight condition registers, which may be selectively set by other instructions. Every conditional branch instruction in a program is coded to refer to one condition register. In most program situations, the appropriate register will be set (and hence the branch decision will be determined) before the branch instruction exits the instruction queue.

If the branch instruction's decision is already determined, either because the instruction's condition register has been set or because it is an unconditional branch, the branch unit removes the branch instruction from the instruction queue and updates subsequent instructions in the instruction queue to conform to the branch. Only in rare cases does the branch instruction pass from the instruction queue to the processing units. Hence in most situations, branch instructions do not require any processing time; they are resolved by modifying the instruction queue while other instructions are being processed.

Processing Units

When an instruction leaves the instruction queue, it goes to one of the **processing units**—either an integer unit or a floating-point unit. The PowerPC 601 microprocessor contains one each; future PowerPC microprocessors will contain multiple integer and floating-point units.

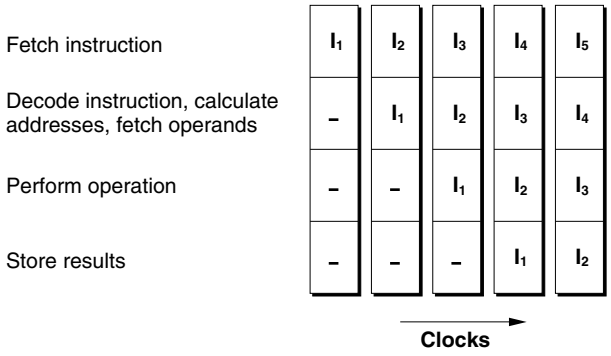
Each processing unit contains four subunits, which process instructions in the following stages:

- fetch the instruction
- decode the instruction; calculate addresses and fetch operands
- perform the operation
- store the results in the data cache

The subunits operate simultaneously, so four instructions pass through a processing unit at a time. During each clock cycle, a different instruction is handled by each subunit. This process, called *pipelining*, is illustrated in Figure A-2, where I_1 through I_5 represent sequential instructions in the program being executed.

Notice in Figure A-2 that the pipelining process takes place with a minimum of idle time. Ideally, the processor never needs to hold up execution of an instruction to wait for the results of a previous instruction. When a program is compiled to run on the PowerPC microprocessor, the compiler tool helps the pipelining process—it arranges the instruction order so that the conditions necessary for each instruction's execution (such as placing required data in the appropriate registers) are satisfied in advance. The ability of RISC processors to execute instructions in parallel paths without halting is the primary reason for their superior performance.

Figure A-2 Instruction pipelining



By taking advantage of pipelining, each processing unit inside the PowerPC microprocessor can execute instructions at the rate of one per clock cycle. With multiple processing units, the processor as a whole can execute more than one instruction per cycle. Because all instructions go through the same processing stages, the only reason the PowerPC microprocessor may need to halt is if a processing unit encounters a branch instruction whose branch condition is not yet set. Under peak conditions, the PowerPC 601 microprocessor can execute three instructions simultaneously—one each in the branch unit, the integer processing unit, and the floating-point processing unit.

In contrast, CISC microprocessors may take up to five clock cycles to execute a single instruction and must also frequently delay processing to determine the results of previous instructions.

Data Cache

The data cache contains 32 general-purpose registers and 32 floating-point registers inside the PowerPC 601 microprocessor chip. Each register has a capacity of 64 bits. The PowerPC instruction set does not process external memory directly; it processes only the contents of its internal registers. Hence external data must be read into registers before processing, and the result must be read back from a register to external memory afterward. This requirement increases program length but greatly accelerates program execution.

Data Organization

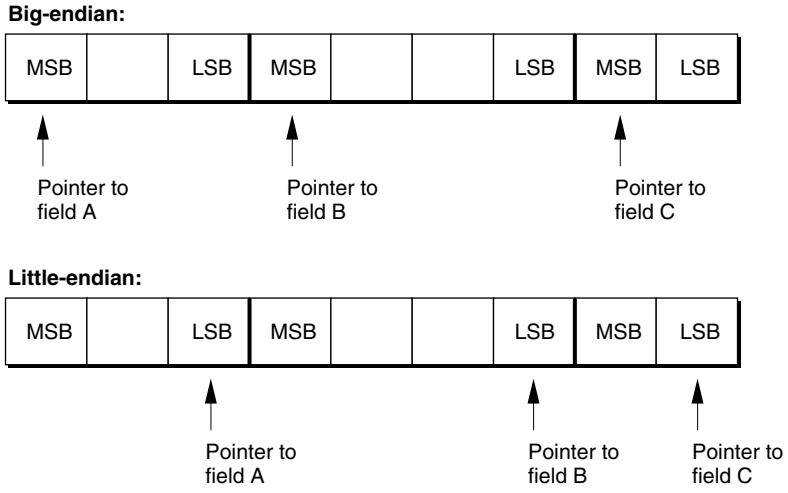
There are two ways that multibyte data fields may be addressed:

- **big-endian** addressing, where the address for the field refers to its most significant byte
- **little-endian** addressing, where the address for the field refers to its least significant byte

Since fields are normally stored in RAM by writing from lower to higher addresses, big-endian addressing also means that the field's lowest address in physical memory contains its most significant byte; little-endian addressing means that the field's lowest address contains its least significant byte.

These two types of data organization are illustrated in Figure A-3, which shows a region of memory containing successive fields that are 3, 4, and 2 bytes long. MSB and LSB indicate the most significant and least significant bytes in each field, respectively.

Figure A-3 Big-endian and little-endian addressing



PowerPC processors and processors of the Motorola 68000 family use big-endian addressing; Intel processors use little-endian addressing. Different I/O chips, accessory card memories, and peripheral devices may use one addressing mode or the other, so data in versatile computing systems such as the Macintosh must often be accessed in either form.

If the Macintosh system always wrote and read multibyte data fields in one operation, it would not matter whether the fields were addressed in big-endian or little-endian mode. For example, if the hardware always transferred an 8-byte field in a single transaction, using 64 bit lines, it would be immaterial whether the location of the field were defined by referencing its most significant byte or its least significant byte.

But when fields are transferred by systems of limited data width, they must often be divided into subfields that fit the system's capacity. When this happens, it is essential to take into account the addressing modes of both the source and destination of the data so that fields can be disassembled and reassembled correctly. One way to convert data from one addressing mode to the other is to reverse the order of bytes within each field, so that a pointer to the most significant byte of a field will point to the least significant byte, and vice versa.

Note
The difference between big-endian and little-endian formats applies only to data; the Macintosh system always transfers addresses as unbroken 32-bit quantities. ◆

It is possible to determine whether a system uses big-endian or little-endian addressing by comparing the way it arranges bytes in order of significance with the way it addresses fields. For example, the following code makes this test:

```
typedef unsigned short  half;
typedef unsigned char   byte;

union {
   half H;
   byte B[2];
   }    halfTrick;
halfTrick ht;
ht.H = 0x2223;
if ( ht.B[0] == 0x22 )
   printf( "I'm big-endian");
else
   printf( "I'm little-endian" );
```

The Macintosh hardware supports both big-endian and little-endian addressing. To accommodate various combinations of source and destination byte formats, PowerPC processor-based Macintosh systems contain two mechanisms that translate between the addressing modes:

- A group of byte-reversed indexed load and store actions are included in the PowerPC instruction set—for example, the `lwbrx` (load word byte-reversed index) instruction. These instructions can convert either big-endian or little-endian data to the other mode, because the two formats are complementary.
- The PowerPC processor supports a little-endian mode that changes the way that real addresses are used to access physical storage. It applies a logical exclusive-OR operation with a constant to the lowest 3 bits of the address, using a different constant for each size of data. This modifies each address to the value it would have if the PowerPC processor used little-endian addressing.

Programs and subsystems that exchange data only internally can usually adopt either big-endian or little-endian addressing without taking into account the difference between the two. As long as they operate consistently they will always store and retrieve data correctly. Systems that exchange data with other devices or subsystems, however, may need to determine the addressing mode of the external system and adapt their data formats accordingly.

When designing expansion cards for Macintosh computers, including their associated software, observe the following general cautions about byte formats:

- The underlying Macintosh hardware generally supports big-endian addressing.
- Most compilers do not provide support for switching data from one addressing mode to another or for using the PowerPC mechanisms that switch modes. Such support can be provided, for example, by a set of C macros that redefine the access mechanisms for basic data types.
- Frame buffers for video, graphics, and sound must support the Macintosh big-endian pixel format. For a discussion of the Macintosh pixel format, see *Inside Macintosh: QuickTime*, listed in "Supplementary Documents," in the preface.

The PowerPC Microprocessor Family

The PowerPC 601 microprocessor used in Power Macintosh computers is the first of a series of PowerPC microprocessor models. The following additional models are currently under development:

- *PowerPC 603:* a low-power, low-cost design for laptop and portable computers, low-cost desktop computers, and personal digital assistants. It will offer performance similar to that of the PowerPC 601.
- *PowerPC 604:* a successor to the PowerPC 601 with more processing units and increased power, for midrange to high-end desktop computers and servers
- *PowerPC 620:* a high-performance microprocessor with full 64-bit architecture for workstations and large-network servers

All PowerPC microprocessors will support the same RISC technology and will be compatible with code written for the PowerPC 601.

Power Macintosh Application Development

The PowerPC 601 microprocessor has a different instruction set from that of the MC68000-family processors that previously powered Macintosh computers. However, the application programming interface (API) for Power Macintosh computers is still based on Macintosh system software version 7.1 and is essentially the same as the API for the Macintosh Quadra 800 and other recent Macintosh computers. The Power Macintosh 6100/60, 6100/60AV, 7100/66, 7100/66AV, 8100/80, and 8100/80AV use identical system software and support the same set of system calls, instructions, and data structures.

This appendix discusses the effect of the PowerPC processor environment on the process of developing application software for Power Macintosh computers.

Building New Software

The presence of the PowerPC 601 processor and its supporting system software in Power Macintosh computers gives you a choice of build processes for new applications:

- You can compile application software as if it were to run on a Macintosh computer containing an MC68000-family processor (for example, any Macintosh Quadra model). In this book, the result is called **68000 code.** When your software is launched, the system software will emulate the run-time environment of a Motorola MC68LC040 microprocessor.
- You can compile new source code (or recompile existing source code) for execution by the PowerPC 601 processor. The result, called **native code,** will run much faster than 68000 code on Power Macintosh computers, but it will not run on previous Macintosh computers.
- You can perform both these build processes, combining 68000 code and native code in an execution module called a **fat binary.** When launched on a Power Macintosh computer, the fat binary runs its native code; when launched on any other Macintosh computer, it runs its 68000 code.

Converting Existing Software

There are several options for adapting existing Macintosh software to run on Power Macintosh computers. They are based on the build options listed in the previous section:

- You can do nothing to the software. If you have followed the guidelines in *Inside Macintosh*, your software compiled for previous Macintosh computers should run as is.
- You can recompile your software into native code, delivering the result either alone or combined with your existing 68000 code in a fat binary.
- You can translate your existing 68000 code into native code directly, without recompiling source text, using translation services provided by third-party vendors.

For information about compiling native code, building fat binaries, and translating 68000 code into native code, see *Building Programs for PowerPC Processor–Based Macintosh Computers*. This book is described in "Supplementary Documents," in the preface.

Application Performance and System Requirements

Each of the software building options described in the previous two sections entails tradeoffs in execution performance, application code size, and system RAM requirements.

By taking advantage of RISC's inherently greater speed, applications written specifically for PowerPC processors run noticeably faster than applications written for other processors, including Pentium. In general, PowerPC processor–based Macintosh systems offer two to four times the performance of today's fastest 68040- and Intel 486–based personal computers. At 66 MHz, the PowerPC 601 processor executes native code at a rate of more than 60 SPEC int92 specmarks and more than 80 SPEC fp92 specmarks. Apple's benchmark tests have found some cases, such as mathematical calculations, in which PowerPC processor–based Macintosh systems ran eight to ten times faster than systems that use other processors.

However, code size tends to increase when an application is recompiled for the PowerPC processor. The increase ranges from negligible to more than double (in the case of a fat binary). A typical increase amount is 20 percent.

Some applications also require more RAM space to hold data when running on a PowerPC processor. This increase is not easily predictable but tends to be small.

System Software Additions

To support the PowerPC processor and provide new functionality, Power Macintosh computers are supplied with a new version of Macintosh System 7.1. The system software installed in ROM and on the internal hard disk contains several new managers in addition to the familiar Macintosh Toolbox. For complete information about these managers, including information about the PowerPC run-time environment, see *Inside Macintosh: PowerPC System Software.* This book is described in "Supplementary Documents," in the preface.

The following is a brief summary of the major additions to the Macintosh Operating System for Power Macintosh computers:

- *Code Fragment Manager.* The Code Fragment Manager is a new part of the Macintosh Operating System that loads fragments into RAM and prepares them for execution. A **fragment** may be an application, a shared library, a system extension, or any other block of executable code and its associated data. The operations of the Code Fragment Manager are loosely analogous to those of the Segment Manager in previous versions of the Macintosh system software.
- *Mixed Mode Manager.* The Mixed Mode Manager is a new part of the Macintosh Operating System that lets Power Macintosh computers run software written for MC68000 computers along with software written for the PowerPC processor. Among its features, the Mixed Mode Manager lets applications written for one platform access and use system software written for the other platform.
- *Exception Manager.* The Exception Manager is a new part of the Macintosh Operating System that handles exceptions that occur during the execution of native PowerPC code. An **exception** is an error or other unusual condition detected by the processor during program execution. The Exception Manager also lets applications install their own exception handlers to supersede some or all of its operations.

For technical information about the rest of the Macintosh System 7.1 software, see *Inside Macintosh.* This suite of books is described in "Supplementary Documents," in the preface.

DOS / Windows Emulation

Insignia Solutions offers SoftWindows, a software product that runs on Power Macintosh computers. It is a successor to SoftPC with Windows and has been designed under license from Microsoft. SoftWindows adds an environment for running applications compatible with Microsoft DOS and Microsoft Windows. It works in approximately the same way as the emulation of 68000 code described in "Building New Software," earlier in this appendix. Further technical information is available from Insignia Solutions.

With SoftWindows installed, the Power Macintosh user can run existing DOS and Windows software in a window on the Macintosh desktop. By choosing items from the application menu at the right end of the Macintosh menu bar, the user can switch instantly between Windows applications, 68000-based Macintosh software, and new PowerPC applications. The Power Macintosh floppy disk drive accepts disks formatted for both DOS and Macintosh environments, and the computer's I/O facilities are available for use by DOS and Windows applications.

Glossary

ADB See **Apple Desktop Bus.**

ADC See **analog-to-digital converter.**

AMIC See **Apple Memory-Mapped I/O Controller.**

analog-to-digital converter (ADC) Circuitry that measures analog electrical levels and delivers the results as digital data.

APDA Apple's worldwide direct distribution channel for Apple and third-party development tools and documentation products.

API See **application programming interface.**

Apple AV Technologies A set of advanced I/O features for Macintosh computers that includes video input and output, sophisticated 16-bit stereo sound input and output, and speech recognition and synthesis.

Apple Desktop Bus (ADB) An asynchronous bus used to connect relatively slow user-input devices to Apple computers.

Apple Memory-Mapped I/O Controller (AMIC) A chip that performs most I/O logic and control for Power Macintosh computers.

AppleTalk Apple's local area networking protocol.

application programming interface (API) A set of calls, instructions, and data structures in system software or a processor instruction set that application software can use to program the computer.

arbitration The process of determining which of several contending subsystems gains control of a bus at any given time.

Ariel II A video chip that provides a color lookup table and digital-to-analog converter for driving a monitor.

AudioVision An Apple monitor design with an interface that combines video, sound, and the ADB in a single cable.

audio waveform amplifier and converter (AWAC) A chip that combines a waveform amplifier with a digital encoder and decoder (codec) for analog sound data, including speech.

AV card A PDS card for Power Macintosh computers that adds 2 MB of VRAM and gives a computer the video I/O features of the Apple AV Technologies. The model numbers of Power Macintosh computers that contain the AV card end in AV.

AWAC See **audio waveform amplifier and converter.**

BART NuBus controller A chip that provides a data gateway between NuBus and the CPU bus in PowerPC processor–based Macintosh systems.

big-endian Data formatting where fields are addressed by pointers to their most significant bytes or bits. See also **little-endian.**

block transfer Data transfers of more than one longword at a time.

branch unit The part of the PowerPC architecture that handles branch instructions, usually without adding any time to program execution.

CAS See **column address strobe.**

CCIR Comité Consultatif International Radio.

CD-ROM See **compact disc ROM.**

CISC See **complex instruction set computing**.

CIVIC See **Cyclone Integrated Video Interfaces Controller.**

CMOS See **complementary metal-oxide semiconductor.**

codec A digital encoder and decoder.

color depth The number of bits required to encode the color of each pixel in a display.

column address strobe (CAS) A signal that captures the column component of a matrix addressing scheme from a bus that carries both row and column addresses.

compact disc ROM (CD-ROM) A read-only data storage disk 120 mm in diameter that can hold up to 550 MB of data.

complementary metal-oxide semiconductor (CMOS) A chip material and fabrication technology that features low power requirements and high noise immunity.

complex instruction set computing (CISC) A technology of microprocessor design in which machine instructions have nonuniform formats and are executed through different processes.

composite video A video signal that includes both picture information (with chroma and luminance combined) and the timing and other signals needed to display it. It is the standard signal form for communication between video-cassette recorders, television sets, and other common video equipment. See also **S-video.**

convolution The process of smoothing alternate lines of a video signal to be shown in succeeding frames for a line-interlaced display.

CPU bus The bus connected directly to the main processor.

Cuda A microcontroller chip that manages the ADB and real-time clock, maintains parameter RAM, manages power on and reset, and performs other general system functions.

Curio An I/O chip that supports Ethernet, SCSI, SCC, and LocalTalk.

Cyclone Integrated Video Interfaces Controller (CIVIC) A video control chip that manages VRAM, generates video timing signals, and performs convolution where needed.

DAC See **digital-to-analog converter.**

data burst Multiple longwords of data sent over a bus in a single, uninterrupted stream.

data cache In the PowerPC architecture, the internal registers that hold data being processed.

data path chip A chip that provides buffering between the cached CPU bus and I/O and DRAM memory accesses.

DAV interface See **digital audio/video interface.**

digital audio/video (DAV) interface A connector on the AV card that lets a NuBus card with a ribbon cable on it access digital sound and unscaled YUV video data directly.

digital-to-analog converter (DAC) Circuitry that produces analog electrical levels in response to digital data.

direct memory access (DMA) A process of transferring data rapidly into or out of RAM without passing it through a processor or buffer.

DMA See **direct memory access.**

DRAM See **dynamic random-access memory.**

dynamic random-access memory (DRAM) Random-access memory in which each storage address must be periodically interrogated ("refreshed") to maintain its value.

Ethernet A high-speed local area network technology that includes both cable standards and a series of communications protocols.

exception An error or other unusual condition detected by a processor during program execution.

facsimile (fax) A data format and transmission protocol for sending graphic images over telephone lines.

fat binary An execution module that contains native code and 68000 code for the same program.

fax See **facsimile.**

floating-point format A data format that stores the magnitude, sign, and significant digits of a number separately.

fragment An application, shared library, system extension, or any other block of executable code and its associated data in a PowerPC processor–based Macintosh system.

GCR See **Group Code Recording.**

Group Code Recording (GCR) An Apple recording format for floppy disks.

high-speed memory controller (HMC) A chip that provides direct memory access between main memory and peripheral devices.

HMC See **high-speed memory controller**.

IEEE Institute of Electrical and Electronics Engineers.

input/output (I/O) Parts of a computer system that transfer data to or from peripheral devices.

instruction queue The part of the PowerPC architecture that holds incoming instructions.

Integrated Services Digital Network (ISDN) A series of protocols that integrate voice and data transmission over telephone lines.

I/O See **input/output.**

ISDN See **Integrated Services Digital Network.**

little-endian Data formatting where fields are addressed by pointers to their least significant bytes or bits. See also **big-endian.**

LocalTalk The cable terminations and other hardware that Apple supplies for local area networking from Macintosh serial ports.

MACE See **Media Access Controller for Ethernet.**

MC68000 The model number of a family of microprocessor chips manufactured by Motorola.

Media Access Controller for Ethernet (MACE) Circuitry within Curio that supports Ethernet I/O.

MFM See **Modified Frequency Modulation.**

Mickey A video encoder that produces composite and S-video outputs in NTSC and PAL formats.

mini-DIN An international standard form of cable connector for peripheral devices.

Modified Frequency Modulation (MFM) A recording format for floppy disks used by DOS computers.

native code Instructions that run directly on the PowerPC processor. See also **68000 code.**

New Age A controller chip for Apple floppy disk drives.

NTSC An acronym for National Television Standards Committee, the television signal format common in North America, Japan, parts of South America, and other regions.

NuBus A bus architecture in Apple computers that supports plug-in expansion cards.

NuBus adapter card A card for the Power Macintosh 6100/60 that gives the computer NuBus capability. It plugs into the PDS connector and accepts short NuBus cards.

PAL An acronym for Phased Alternate Lines, the television signal format common in Western Europe (except France), Australia, parts of South America, most of Africa, and Southern Asia.

PBX See **Private Branch Exchange.**

PDS See **processor-direct slot.**

pipelining The technique of sending instructions through multiple processing units in such a way that each unit handles one instruction per clock cycle.

pixel Contraction of *picture element*; the smallest dot that can be drawn on a display.

PowerPC Tradename for a family of RISC processors. The PowerPC 601 is used in Power Macintosh computers.

Private Branch Exchange (PBX) The traditional transmission standard for voice telephone.

processing unit A part of the PowerPC architecture that executes instructions, using the pipelining technique.

processor-direct slot (PDS) A connector that lets a plug-in card access the CPU bus directly. A PDS connector can accept a NuBus adapter card, an Apple video card, or a third-party card.

RAS See **row address strobe.**

reduced instruction set computing (RISC) A technology of microprocessor design in which all machine instructions are uniformly formatted and are processed through the same steps.

RGB Abbreviation for *red-green-blue*. A data format for color displays in which the red, green, and blue values of each pixel are separately encoded.

RISC See **reduced instruction set computing.**

row address strobe (RAS) A signal that captures the row component of a matrix addressing scheme from a bus that carries both row and column addresses.

RS-232, RS-422 Standard communications protocols established by the Electronics Industries Association for serial data transmission.

SCC See **Serial Communications Controller.**

SCSI See **Small Computer System Interface.**

Sebastian A video color manager and digital-to-analog converter on one chip.

SECAM A French acronym for the television signal format used in France, Eastern Europe, the former Soviet Union, and many former French colonies.

Serial Communications Controller (SCC) Circuitry on the Curio chip that provides an interface to the serial data ports.

SIMM See **Single Inline Memory Module.**

Single Inline Memory Module (SIMM) A plug-in card for expanding RAM that contains several RAM chips and their interconnections.

68000 code Instructions that can run on the PowerPC processor only through an emulator. See also **native code.**

Small Computer System Interface (SCSI) An industry standard parallel bus protocol for connecting computers to peripheral devices such as hard disk drives.

Squidlet A clock chip used in Power Macintosh computers.

SuperDrive Apple Computer's disk drive for high-density floppy disks.

S-video A video format in which chroma and luminance are transmitted separately. It provides higher image quality than **composite video.**

SWIM III A controller chip for the Apple SuperDrive floppy disk drive.

TrueColor Apple's color encoding system using 24 bits per pixel for color information.

Versatile Interface Adapter (VIA) The interface for system interrupts that is standard on most Apple computers.

VIA See **Versatile Interface Adapter**.

video frame buffer Memory that stores one or more frames of video information to be displayed on a screen.

video RAM (VRAM) Random-access memory used to store both static graphics and video frames.

VRAM See **video RAM**.

VRAM expansion card A PDS card that adds second monitor support with 2 MB or 4 MB of VRAM to the Power Macintosh 7100/66 or 8100/80.

YUV A data format for each pixel of a color display in which color is encoded by values calculated from its native red, green, and blue components.

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